UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

TQ DELTA, LLC, Plaintiff, v. 2WIRE, INC., Defendant.	Civil Action No. 13-cv-1835-RGA
TQ DELTA, LLC, Plaintiff, v. ZHONE TECHNOLOGIES, INC., Defendant.	Civil Action No. 13-cv-1836-RGA
TQ DELTA, LLC, Plaintiff, v. ZYXEL COMMUNICATIONS, INC., and ZYXEL COMMUNICATIONS CORPORATION, Defendants.	Civil Action No. 13-cv-2013-RGA
TQ DELTA, LLC, Plaintiff, v. ADTRAN, INC., Defendant.	Civil Action No. 14-cv-954-RGA
ADTRAN, INC., Plaintiff, v. TQ DELTA, LLC, Defendant.	Civil Action No. 15-cv-121-RGA

PARTIES' JOINT CLAIM CONSTRUCTION
BRIEF FOR THE FAMILY 3 PATENTS

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I. INTRODUCTION

A. Plaintiff's Position

Pursuant to the Third Scheduling Order, Plaintiff TQ Delta, LLC. ("TQD") submits its Opening Claim Construction Brief for the Family 3 Patents. TQD submits that its proposed constructions are supported by the claim language, intrinsic record, and strong extrinsic evidence, and should therefore be adopted by the Court. In contrast, Defendants proposed constructions rewrite the claims to import additional limitations or, in some instances, to render the scope of the claim ambiguous.

B. Defendants' Answering Position

The Family 3 patents[1] relate to allocating shared memory used by a DSL transceiver. During prosecution of the parent application in the family, the examiner identified only a single feature as possibly novel over the prior art: the content of the claimed message specifying the maximum number of bytes available to be allocated. *See* A180 (D.I. 312, Ex. H). As such, any alleged point of novelty for the Family 3 patents is very narrow, and the asserted claims of the Family 3 patents should be construed accordingly.

TQ Delta's proposed constructions improperly seek to broaden the claims to cover plainly non-infringing technology. For example, TQ Delta tries to relax the claims' requirement that the message specify a number of bytes to be allocated to an interleaver and or a deinterleaver function, based solely on extrinsic evidence and the unsupported statements of its experts. TQ Delta's approach and its constructions should be rejected. *See Impulse Tech. Ltd. v. Microsoft Corp.*, No. CV 11-586-RGA-CJB, 2015 WL 1737663, at *4 (D. Del. Apr. 9, 2015)

[1] "Family 3" consists of U.S. Patent Nos. 7,831,890 ("the '890 patent"), 7,836,381 ("the '381 patent"), 7,844,882 ("the '882 patent"), 8,276,048 ("the '048 patent"), 8,495,473 ("the '873 patent") and 8,607,126 ("the '126 patent"). The Family 3 patents share a common specification; citations are to the '890 patent unless otherwise noted.

("'conclusory, unsupported assertions by experts as to the definition of a claim term are not useful to a court[,]' and are to be afforded less weight in a claim construction analysis than are citations to the intrinsic record."), report and recommendation adopted, No. 11-586-RGA, 2015 WL 5568616 (D. Del. Sept. 22, 2015), aff'd, 665 F. App'x 872 (Fed. Cir. 2016).

Defendants' proposed constructions should be adopted because they are consistent with the purpose and scope of the alleged invention, the context of the claims in which the disputed terms appear, and are amply supported by the intrinsic evidence. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1316 (Fed. Cir. 2005) ("The construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction.").

In addition, several of the asserted claims are indefinite under 35 U.S.C. § 112, ¶ 2 because "a person of ordinary skill in the art would be unable to tell if the apparatus itself would infringe or if the apparatus would have to be used in a certain way to infringe." *Sound View Innovations, LLC v. Facebook, Inc.*, No. 16-cv-116, 2017 WL 2221177, at *8 (D. Del. May 19, 2017) (Andrews, J.) (discussing *IPXL Holdings, Inc. v. Amazon.com Inc.*, 430 F.3d 1377, 1384 (Fed. Cir. 2005)). A claim must be construed "as written, not as the patentees wish they had written it." *Chef Am., Inc. v. Lamb-Weston, Inc.*, 358 F.3d 1371, 1374 (Fed. Cir. 2004).

C. Plaintiff's Reply Position

Pursuant to the Third Scheduling Order, Plaintiff TQ Delta, LLC. ("TQD") submits its Reply Claim Construction Brief for the Family 3 Patents. TQD submits that its proposed constructions are supported by the claim language, intrinsic record, and strong extrinsic evidence, and should therefore be adopted by the Court. In contrast, Defendants proposed constructions rewrite the claims to import additional limitations or, in some instances, to render the scope of the claim ambiguous.

D. Defendants' Sur-reply Position

Once again, TQ Delta's claim construction briefing overemphasizes extrinsic evidence and improperly minimizes the intrinsic evidence. TQ Delta submits and relies on yet another conclusory declaration from its expert to interpose concepts (such as "memory cells") that appear nowhere in the intrinsic record. *See, e.g., Network Commerce, Inc. v. Microsoft Corp*., 422 F.3d 1353, 1361 (Fed. Cir. 2005) (disregarding expert declaration where expert "[did] not support his conclusion with any references to industry publications or other independent sources").[2] TQ Delta repeatedly argues that the teachings of the specification should be disregarded, often by relying on pre-*Phillips* cases, in an effort to broaden certain claim terms. TQ Delta also argues that the prosecution history – which unambiguously shows that the only potential point of novelty is the content of the message allocating shared memory – should be disregarded. TQ Delta's approach turns proper claim construction on its head, and should be rejected.

By contrast, Defendants' constructions are rooted firmly in the intrinsic evidence, reflect the proper scope of the invention as understood by a person of ordinary skill in the art, and should be adopted by the Court.

II. DATA COMMUNICATIONS

A. Plaintiff's Position

Data communication between two communication endpoints, a first and second transceiver for example, is effected by communicating one or more bits of data (data bits)

[2] *See also, e.g., Eleven Eng'g, Inc. v. Microsoft Corp*., No. CV 09-903-LPS, 2016 WL 3457190, at *3 (D. Del. June 23, 2016), aff'd, No. 2016-2439, 2017 WL 3049604 (Fed. Cir. July 19, 2017); *Wireless Agents LLC v. Sony Ericsson Mobile Commc'ns AB*, 189 F. App'x 965, 968 (Fed. Cir. 2006) (finding that expert's statement was "conclusory and is unsupported by reference to any contemporaneous document and therefore of no value in [the court's] claim construction analysis"); *Intelligent Computer Sols., Inc. v. Voom Techs., Inc*., 509 F. Supp. 2d 847, 862 (C.D. Cal. 2006) (affording "little weight" to expert assertions made "without relying on independent sources or analysis of industry publications").

serially. A676 (Cooklev Decl.) at ¶ 11. The data bits are communicated over a communication medium that may be, for example, a phone line. *Id*. In one exemplary scheme, bits of data are communicated serially in the form of a bit stream. *Id*. In another exemplary scheme, DMT for example, groups of bits of data are communicated serially. *Id*. An illustration of a bit stream is shown below. *Id*. Each white box represents a single bit or a group of data bits. *Id*.

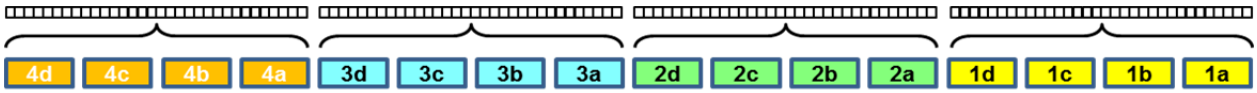
1. Errors in Communicated Data

Bits of data communicated over a communication medium may be corrupted by noise. A678 (Cooklev Decl.) at ¶ 15. Noise is defined as "unwanted disturbances superimposed upon a useful signal that tend to obscure its information content." A84 (IEEE 100 The Authoritative Dictionary of IEEE Standards Terms, 7th ed. (2000) at p. 539); A678 (Cooklev Decl.) at ¶ 15. Thus, bits of data transmitted over a communication medium in the presence of noise may not be correctly received. *Id*. One type of noise is impulse noise. Impulse noise is defined as noise that is "characterized by transient disturbances separated in time by quiescent intervals." A82 (IEEE 100 The Authoritative Dictionary of IEEE Standards Terms, 7th ed. (2000) at p. 732); A681 (Cooklev Decl.) at ¶ 21. Impulse noise is typically short in duration and has the effect of randomly corrupting a short sequence of bits of serially transmitted data. A682 (Cooklev Decl.) at ¶ 23. As a result, random sequences of bits may not be correctly received. *Id*.

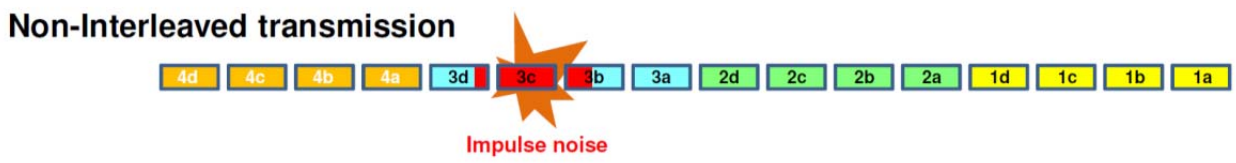
2. Error Correction

To reduce the negative impact of noise, error correction schemes may be used. A679 (Cooklev Decl.) at ¶ 17. For example, groups of data bits may be encoded into corresponding sets of codewords prior to transmission. A680 (Cooklev Decl.) at ¶ 18. The encoding method used is one that allows a group of data bits to be recovered from its corresponding codeword. *Id*.

The figure below illustrates the groupings of data bits and the corresponding codeword generated from each group. *Id*. The codewords are generated using a suitable encoding scheme, Reed Solomon for example. *Id*. In place of the data bits themselves, the groups of data bits in each codeword are then transmitted sequentially over the communication medium. *Id*. Codewords would also typically be communicated sequentially, for example as illustrated below, a yellow codeword, followed by a green codeword, followed by a blue codeword and finally followed by an orange codeword. *Id*.



If one or more bits from a codeword are corrupted by noise, the receiving endpoint may nevertheless be able to recover all of the original data bits using the portions of the codeword that are correctly received. A681 (Cooklev Decl.) at ¶ 21. To allow recovery of the original data bits from a codeword, a minimum or threshold number (or percentage) of bits from the codeword must be correctly received. *Id*. If, however, more than a threshold number of bits from the codeword are corrupted by noise, the original data bits represented by a codeword will not be recoverable. *Id*. This minimum or threshold number is a function of the level of encoding performed when translating the group of data bits to the codeword. *Id*. The level of encoding determines the size of the codewords. Increasing the encoding increases the size of the codewords, however it also decreases the threshold number of bits of a codeword that must be correctly received to recover the original data bits.



Because impulse noise involves short, intermittent bursts, a number of consecutive bits spanning one or more groups of bits in a codeword may be corrupted while other adjacent bits are received correctly (corrupted bits are shaded in red in the illustration above). A681-A682 (Cooklev Decl.) at ¶ 22. If the duration of the impulse noise is sufficiently long, then more than a threshold number of bits of a codeword (for example, more than one quarter or 25% of the bits in a codeword) may be corrupted, which would make it impossible to recover the data bits corresponding to that codeword. *Id*. In the example illustrated above, portions of the blue codeword (all of bits in group 3 and some of the bits of groups 2 and 4 totaling about 40% of the bits of the blue codeword) are corrupted by impulse noise. *Id*. In this example where the threshold is 25%, it would be impossible to recover the original group of data bits that were used to generate the blue codeword. *Id*.

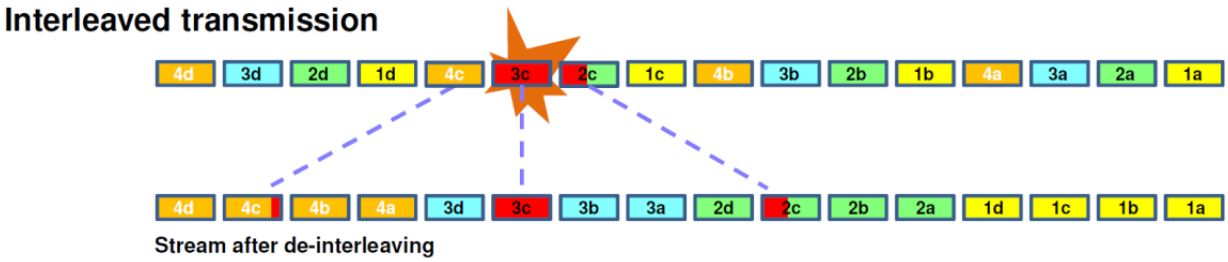
3. Interleaving and Deinterleaving

An improvement to the above-described error correction scheme spreads the impact of impulse noise across multiple codewords. A682 (Cooklev Decl.) at ¶ 23. This approach involves manipulating multiple codewords by rearranging the order in which groups of bits of the multiple codewords are transmitted. *Id*. Groups of bits of a codeword, that otherwise would have been contiguous (i.e., transmitted sequentially), are rearranged so that once contiguous groups of bits of a codeword are now spaced further apart from each and interspersed with groups of bits from a number of other codewords. *Id*. The process of rearranging the order in which groups of bits from multiple codewords are transmitted is called interleaving. *Id*. Because impulse noise is short in duration, spreading out portions of codewords in time ensures that any impulse noise will tend to corrupt a smaller number of bits from any given codeword. *Id*. The collection of multiple codewords that are interleaved may be referred to as a block. *See*

A9 ('890 Patent) at 7:18-20. The size of the block is determined the size of each codeword and the number of codewords in the block. A682 (Cooklev Decl.) at ¶ 23. The number of codewords in the block is referred to as the interleaver depth. *Id*. Increasing the number of codewords in the block, i.e., increasing the interleaver depth, has the effect of spreading the noise over more codewords. *Id*. This allows the receiver to "correct a burst of errors" of a longer duration. *See, e.g.*, A9 ('890 Patent) at 6:20-56. This relationship between interleaver depth and "error correction capability" is set forth in the Family 3 Patents. *See, e.g.*, A9 ('890 Patent) at 6:20-56.

Upon receipt of the complete block of interleaved codewords, the codewords are reassembled by rearranging the groups of bits of the codewords back into their original order. A682 (Cooklev Decl.) at ¶ 24. The process of reordering to reassemble the original codewords is referred to as deinterleaving. *Id*.

The illustration below depicts an interleaved data stream consisting of four groups of bits from four different codewords. A682-A683 (Cooklev Decl.) at ¶ 25. In particular, a first group of bits from each of four different codewords (yellow 1a, green 2a, blue 3a and orange 4a) is first transmitted; then a second group of bits from each codeword (yellow 1b, green 2b, blue 3b, and orange 4b) is transmitted and so on. *Id*. As shown, impulse noise corrupts more than 25% of the total number of bits in the third group of bits. *Id*. However, once the data stream is deinterleaved so that the original codewords are reassembled, the effect of impulse noise is spread across multiple codewords and no individual codeword has more than 25% of its bits corrupted. This would allow the error correction code to recover all of the original data bits. *Id*.



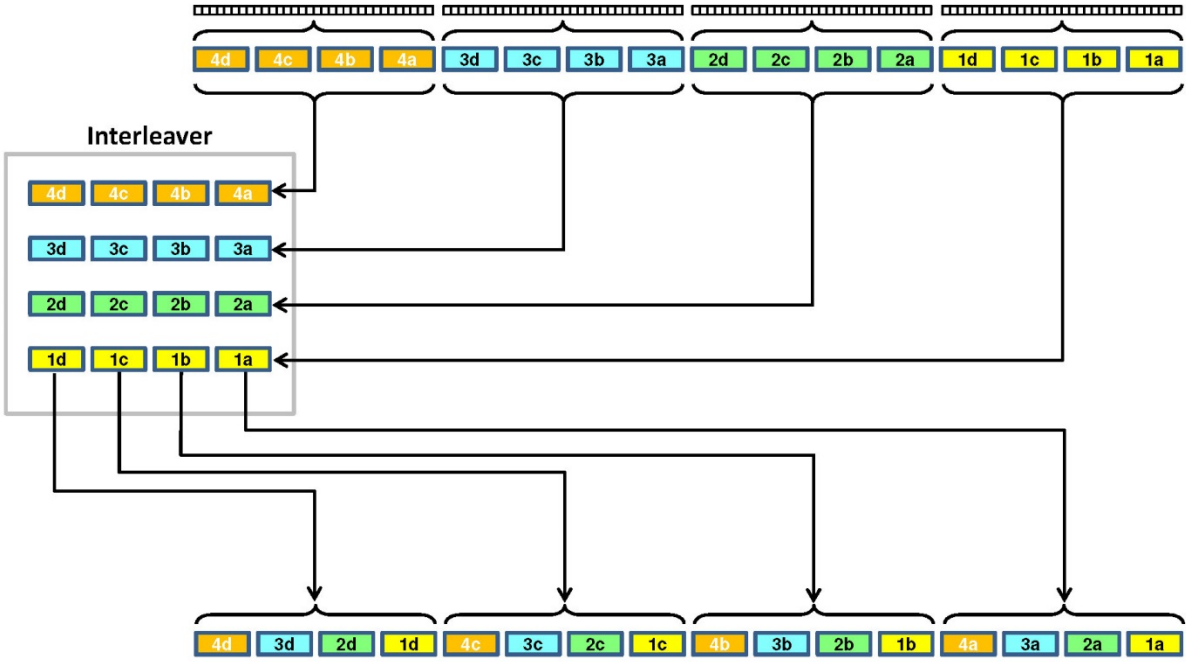
4. Interleaving Latency

Prior to deinterleaving and reassembling codewords at a receiver, all of the groups of bits of a codeword, which have been spread out over time (i.e., the block of interleaved codewords), must be received. A683-A684 (Cooklev Decl.) at ¶ 27. The first-received groups of bits of a codeword must be temporarily stored while waiting for the remaining groups of bits of the codeword to be received. *Id*. For example, in the illustration above, the first group of yellow bits (yellow 1a) must be stored while waiting for the second (yellow 1b), third (yellow 1c), and fourth group (yellow 1d) of yellow bits to be received. *Id*. Only after receipt of all of the bits of a codeword can the codeword be decoded. *Id*. This delays the recovery of the original data bits. *Id*. The time delay that is introduced because of the interleaving/deinterleaving operation is referred to as the latency. *Id*. Latency is a function of the block size i.e., the number of bits in a codeword (i.e., "codeword size") and the number of codewords that are interleaved together (i.e., "interleaver depth"). *Id*. Increasing the codeword size and/or interleaver depth increases the error correction capability of the system, but also increases the latency. *See, e.g.*, A8 ('890 Patent) at 6:20-55.

5. Interleaver

An interleaver is a component in a transceiver that accepts groups of bits of codewords, i.e., a block of codewords, and returns the identical groups of bits but in an order different from the order in which the groups of bits were received. A684 (Cooklev Decl.) at ¶ 28. An example

of a simple interleaver is illustrated below in which each group of bits in each codeword is sequentially written into an interleaver memory row by row. *Id*. The order of transmission of the groups of bits is then rearranged by reading out the groups of bits column by column. *Id*.

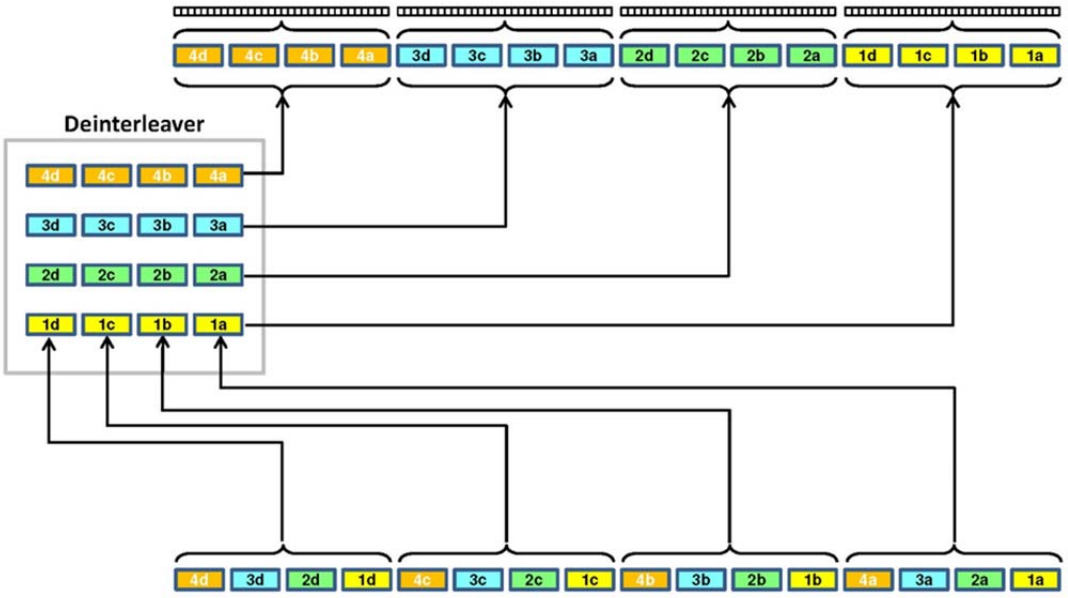


An important element of the interleaver is the interleaver memory that is used to perform the interleaving. A684-A685 (Cooklev Decl.) at ¶ 29. As recognized by the Family 3 Patent specification, the size of the interleaver memory needed to perform the interleaving is determined by the number of codewords being interleaved together in one block (i.e., the interleaver depth), and the size of the individual codewords. *Id*. Increasing the size of the block increases the error correction capability of the system, but also increases the amount of memory required to perform the interleaving operation. *Id*.

6. Deinterleaver

A deinterleaver is a component in a transceiver that receives a block of interleaved codewords, and reassembles the individual codewords of the block by rearranging the groups of

bits of the codewords back into their original order. A685 (Cooklev Decl.) at ¶ 31. The deinterleaved codewords may then be decoded to recover the original data bits. An example of a simple deinterleaver is illustrated below. *Id*. The received block of interleaved codewords is sequentially written into a deinterleaver memory column by column and rearranged by reading out the groups of bits row by row. *Id*.



An important element of the deinterleaver is the memory that is used to perform the deinterleaving. As recognized by the Family 3 Patent specification, the size of the deinterleaver memory needed to perform the deinterleaving is determined by the size of codewords being deinterleaved (i.e., the deinterleaver depth), and the size of the individual codewords. Increasing the size of the block increases the error correction capability of the system, but also increases the amount of memory required to perform the deinterleaving operation. A686 (Cooklev Decl.) at ¶ 33.

7. Transceiver

A transceiver includes a transmitter and a receiver. Consequently, such a transceiver that uses interleaving and deinterleaving includes both an interleaver and a deinterleaver. A685-A686 (Cooklev Decl.) at ¶ 32. The interleaver is used to interleave blocks of codewords prior to transmission and the deinterleaver is used to deinterleave received blocks of interleaved codewords. A680; A685-A686 (Cooklev Decl.) at ¶¶ 18 and 32. The exemplary transceiver illustrated in Figure 1 of the '890 Patent (reproduced below) includes two interleavers 216, 226 and two deinterleavers 316, 326.

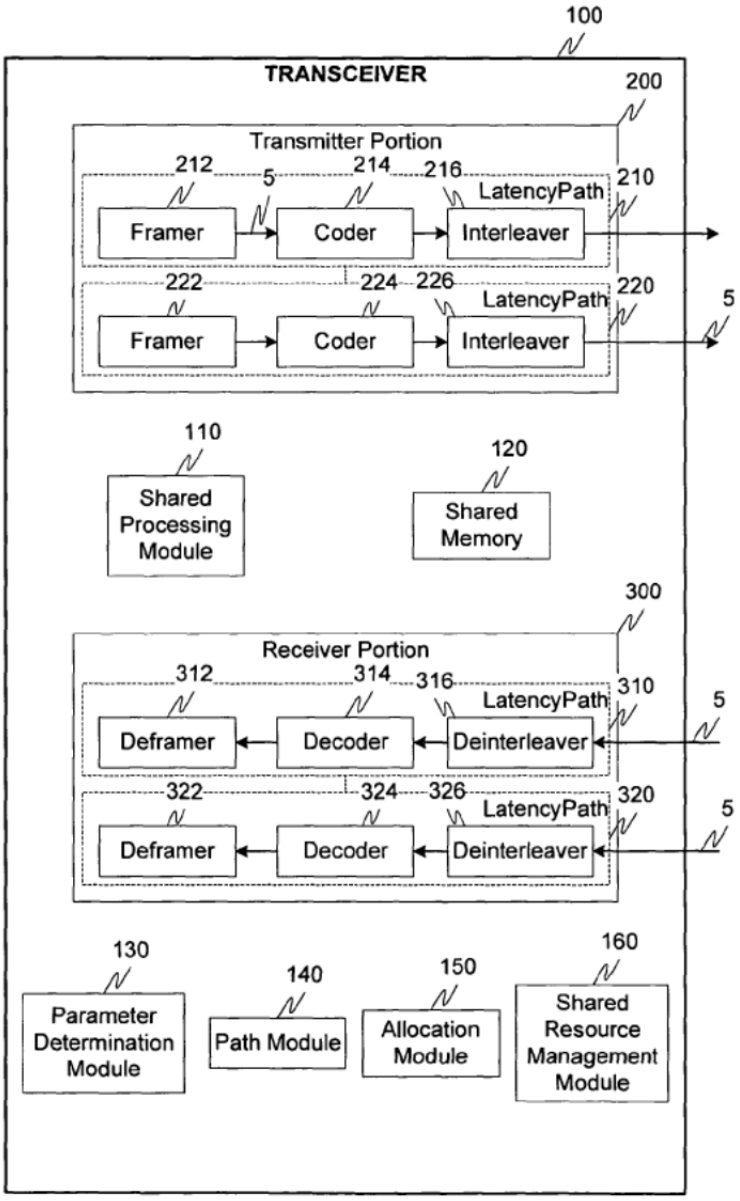


Fig. 1

A3 ('890 Patent) at Fig. 1.

B. Defendants' Position

Defendants generally agree with TQ Delta's high-level discussion of data communications. Defendants simply point out that all of the concepts discussed in this section of TQ Delta's opening brief were well-known in the art prior to the invention date of the Family 3 patents. For example, the use of interleaving and deinterleaving as "[a]n improvement" to

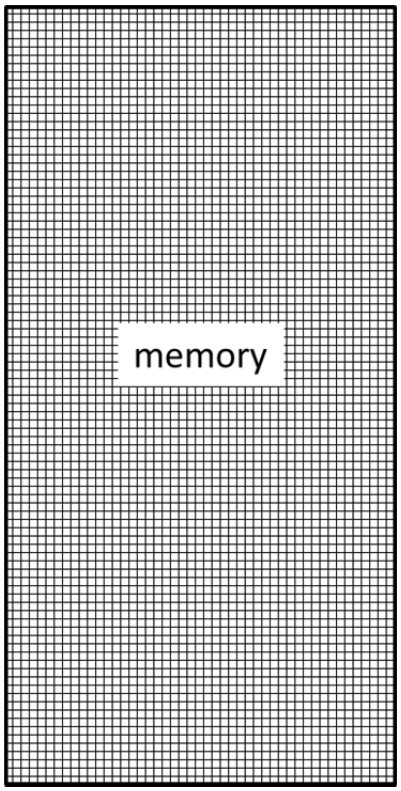
previous error correction schemes (*supra* at p. 6) was well known, as were the tradeoffs between error correction capabilities and latency (delay). A721 (Jacobsen Decl.) at ¶ 17; A6 ('890 patent) at 1:20-39 ("Description of Related Art"). Also well-known at the time were forward error correction schemes in general, and encoding schemes such as Reed-Solomon encoding. A720-A721 (Jacobsen Decl.) at ¶ 16. As discussed below, during prosecution of the Family 3 patents, the Examiner recognized that allocating shared memory between interleavers and deinterleavers in transceivers was also well known. A722-A723 (Jacobsen Decl.) at ¶ 21.

III. SUMMARY OF THE FAMILY 3 PATENTS

A. Plaintiff's Position

Inventions described and claimed by the Family 3 Patents relate to "memory sharing in communication systems." A6 ('890 Patent) at 1:16-17. Specifically, the Family 3 Patents describe schemes to allocate shared memory between an interleaver and a deinterleaver of a transceiver. Memory is used to store information. A89-A90 (IEEE Standard Dictionary of Electrical and Electronics Terms, 4th ed. (1988) at p. 582 ("memory. *See*: storage") and p. 956 (defining storage as "[a]ny device in which information can be stored, sometimes called a memory device") (emphasis added)); *see also* A100-A101 (Standard Dictionary of Computers and Information Processing, Martin H. Weik, 3rd printing (1970) at p. 186 (stating that memory is same as storage) and p. 271 (defining storage as "[a] device . . . which receives data, holds and, at a later time, returns data."); A686-A687 (Cooklev Decl.) at ¶ 35. The interleaver and the deinterleaver of the transceiver each use all or a portion of its allocation of shared memory to perform interleaving and deinterleaving, respectively. A688 (Cooklev Decl.) at ¶ 37. Memory is comprised of memory cells. "A memory cell is the smallest subdivision of a memory into which a unit of data has been or can be entered, in which it is or can be stored, or from which it can be retrieved." A83 (IEEE 100 The Authoritative Dictionary of IEEE Standard Terms, 7th ed.

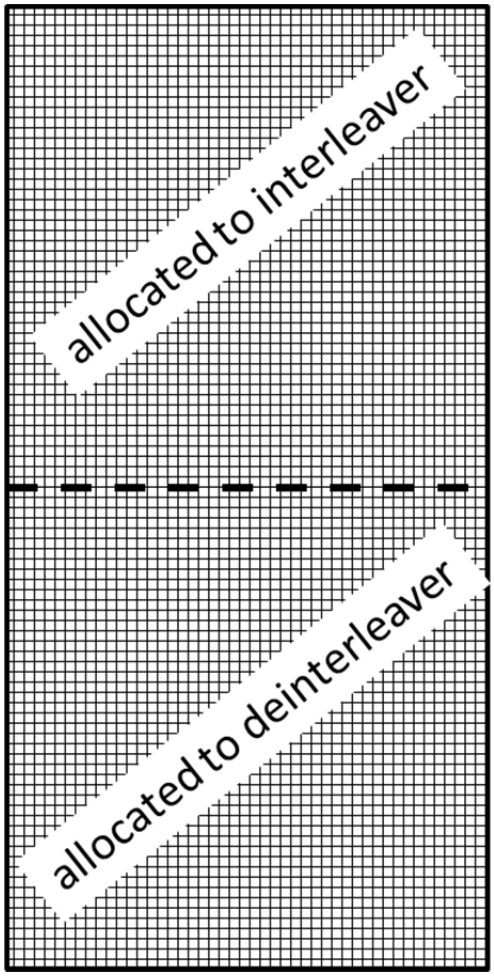
(2000) at p. 685 (defining memory cell as "[t]he smallest subdivision of a memory into which a unit of data has been or can be entered, in which it is or can be stored, and from which it can be retrieved."); *see also* A686-A687 (Cooklev Decl.) at ¶ 35. Shown below is an illustration of memory. Each cell of the grid corresponds to an exemplary memory cell.



In the context of the Family 3 Patents shared memory is memory that can be allocated for use by one or more interleavers and one or more deinterleavers of a transceiver. A688-A689 (Cooklev Decl.) at ¶ 38. The Family 3 Patents explain that the allocation may be performed after the transceiver exchanges messages that "contain information on the total and/or shared memory capabilities of each transceiver and optionally information about the one or more latency paths." A7 ('890 Patent) at 4:23-28; *see also* A690-A691 (Cooklev Decl.) at ¶ 41. For example, based on the received messages, the transceiver may allocate a first portion of the shared memory for

use by an interleaver and allocate a second portion of the shared memory for use by a deinterleaver. A690-A691 (Cooklev Decl.) at ¶ 41.

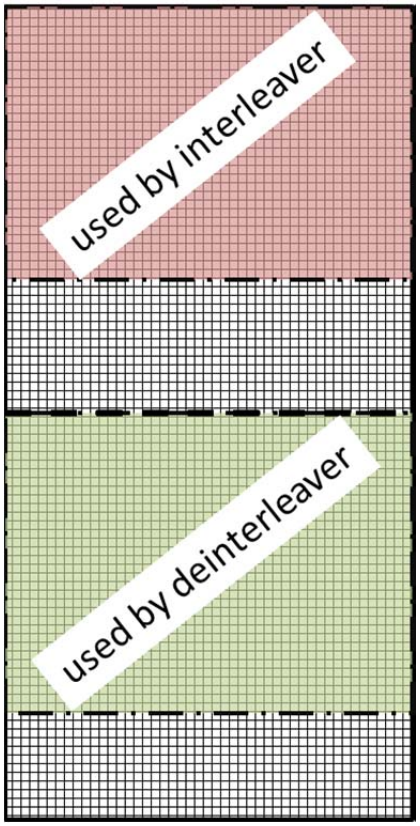
The portion of the shared memory allocated to the interleaver can be used at the same time as the portion of the memory allocated to the deinterleaver. For example, the interleaver may be using a portion of the shared memory to store bits from codewords that are being interleaved at the same time that the deinterleaver is using a portion of the shared memory to store bits from codewords that are being deinterleaved. *See* A35 ('882 patent) at claim 13 ("wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver."); *see also* A689 (Cooklev Decl.) at ¶ 39. The figure below illustrates an example allocation of the shared memory between an interleaver and a deinterleaver. A688-A689 (Cooklev Decl.) at ¶ 38. The portion of shared memory above the dashed line is allocated for use by the interleaver and the portion of shared memory below the dashed line is allocated for use by the deinterleaver. *Id*.



The interleaver uses memory cells from the portion of shared memory allocated to interleaving and the deinterleaver uses memory cells from the portion of shared memory allocated to deinterleaving. As explained in the Family 3 Patent specification, the size of the individual codewords, Reed Solomon codewords for example, and the number of such codewords that are interleaved together determine the amount of the memory allocated to interleaving/deinterleaving that is actually used for the interleaving/deinterleaving operation. A8 ('890 patent) at 6:25-31 ("Reed Solomon coding using a codeword size of 255 bytes (N=255) with 16 checkbytes (R = 16) and interleaving/deinterleaving using an interleaver depth of 64(D=64). This latency path will require N*D = 255*64 = 16Kbytes of interleaver memory at the transmitter (or de-interleaver memory at the receiver)."); A686 (Cooklev Decl.) at ¶ 34. In

other words, the interleaver or deinterleaver may actually use less memory than the amount of shared memory allocated to the function. *See* A689-A690 (Cooklev Decl.) at ¶ 40.

The figure below illustrates the allocation of shared memory used by the interleaver and the interleaver. The pink and green shaded areas of the shared memory indicate the memory cells of the shared memory actually used by the interleaver and deinterleaver, respectively. *See* A689-A690 (Cooklev Decl.) at ¶ 40.



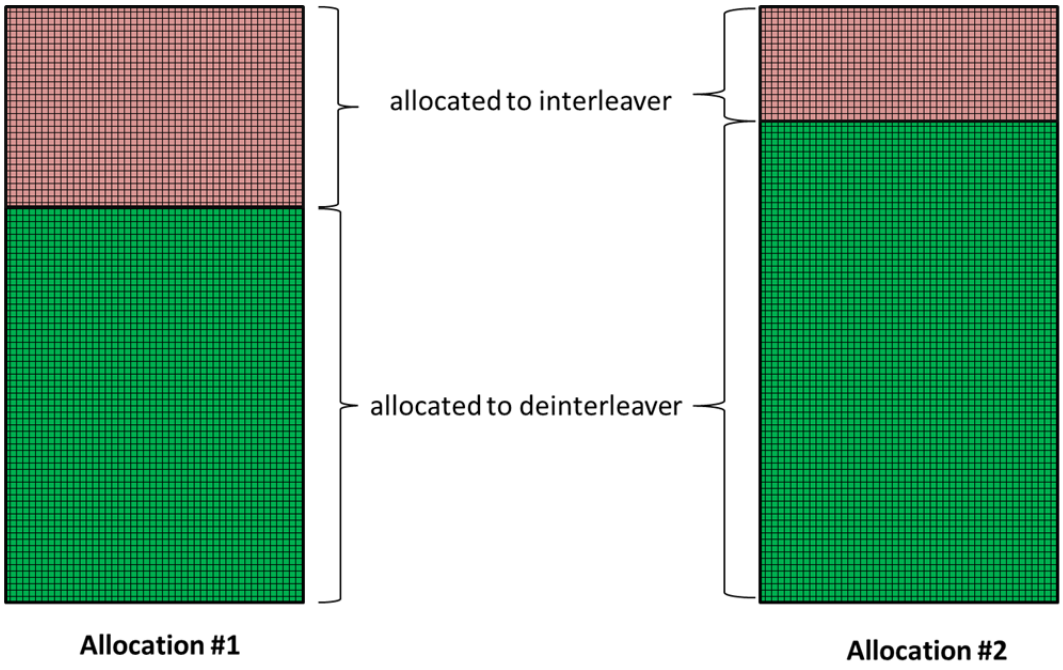
The Family 3 Patent specification explains that the allocation of shared memory between the interleaver and deinterleaver is not fixed. *See* A691 (Cooklev Decl.) at ¶ 42. Instead, "the sharing of resources can be modified and messages transmitted between [] two transceivers at any time during initialization and/or user data transmission." A7 ('890 Patent) at 4:37-40; *See also* A691 (Cooklev Decl.) at ¶ 42. In other words, the messages exchanged between the transceivers are used to coordinate initial allocation, and any subsequent changes in the

allocation, of shared memory. *See* A9 ('890 patent) at 7:54-60 ("This information may need to be forwarded during initialization in order to initially configure the DSL connection. This information may also need to be forwarded during SHOWTIME in order to reconfigure the DSL connection based on a change in applications or the application requirements."); *See* A691 (Cooklev Decl.) at ¶ 42.

The allocation may be adjusted in response to "a change in communication that would require the adjustment of the shared resource allocation." A10 ('890 Patent) at 9:29-32. "Examples of changes in communications conditions include a change in applications being transported over the system and/or changes in the channel condition, etc." A10 ('890 Patent) at 9:32-34. The Family 3 Patent specification explains that applications like "video typically requires a low BER [bit error rate] (<1E-l0) but can tolerate higher latency (>20 ms). Voice, on the other hand, typically requires a low latency (<1 ms) but can tolerate BER (> lE-3)." A6 ('890 Patent) at 1:27-30. Thus, if the application being received by the transceiver changes from voice to video, the far end transceiver may increase the interleaving and level of encoding to account for the low tolerance of video to errors. A691 (Cooklev Decl.) at ¶ 43. This results in an increase in interleaving depth. In this case, the transceiver will need to increase the size of its deinterleaver memory. A691 (Cooklev Decl.) at ¶ 43.

Increasing the size of the deinterleaver memory may require a new allocation of memory so that portions of the shared memory that were previously used by the interleaver are now used by the deinterleaver. A692 (Cooklev Decl.) at ¶ 44. Thus, one or more memory cells that had been allocated to the interleaver may be used by the deinterleaver. *Id.* Such a change in allocation is illustrated below. *Id*. On the left (Allocation #1), a first allocation is shown with about 35% of the memory cells allocated to the interleaver and about 65% allocated to the

deinterleaver. *Id*. On the right (Allocation #2), a different allocation is shown with about 20% of the memory cells allocated to the interleaver and about 80% allocated to the deinterleaver. Per this example, about 15% of the memory cells that were at one time allocated to the interleaver are at another time allocated to the deinterleaver. *Id*.



B. Defendants' Position

The Family 3 patents' specification states that "[o]ne difficulty with implementing multiple latency paths in a transceiver is the fact that a latency path is a complicated digital circuit that requires a large amount of memory" and "[a]n interleaver within a latency path can consume a large amount of memory in order to provide error correcting capability." *See* A6 ('890 patent) at 1:43-54.

The specification asserts that "as the number of latency paths increase, the memory and processing power requirements for a communication system become larger." *Id.* at 1:52-54. In response, the specification describes "sharing memory between one or more interleavers and/or deinterleavers in a transceiver," *id.* at 1:56-57, and discloses providing a message that describes

the maximum number of bytes of memory available to be allocated to an interleaver or deinterleaver function. A8 ('890 patent) at 6:4-11; *see also* A4 ('890 patent) at Fig. 3 and A9 ('890 patent) at 8:65-67.

The point of novelty identified during prosecution of the '890 patent (the parent application in Family 3) was a transmitted message containing information on the maximum number of bytes available to be allocated to an interleaver or deinterleaver. All 45 original claims were rejected under 35 U.S.C. 102(e) as being anticipated by Fadavi-Ardekani (U.S. Patent No. 6,707,822). *See* A150-151 (D.I. 312, Ex. H). The examiner found, for example, that Fadavi-Ardekani teaches methods and systems for "sharing resources in a transceiver" comprising "allocating a first portion of shared memory to a first latency path (i.e., 16 Kbytes is allocated for interleave, lines 25-30 in column 7) and allocating a second portion of the shared memory to a second latency path (i.e., 4 Kbytes is allocated for deinterleave, lines 25-30 in column 7)." A150, 152, 154-55 (D.I. 312, Ex. H). The examiner also found that Fadavi-Ardekani teaches transmitting or receiving "information that is used to determine a maximum amount of shared memory that can be allocated." A151, 156 (D.I. 312, Ex. H). Finally, the examiner found that Fadavi-Ardekani also teaches that the first latency path may include an interleaver and the second latency path may include either a second interleaver or a deinterleaver. A152, 155 (D.I. 312, Ex. H).

In an interview, "[t]he examiner and applicant discussed an overview of the invention and explained features of simultaneous transfer and types of interleaving and allocation of memory based on direction of transmission and bandwidth," and the examiner suggested that the applicant provide more details "such as type of memory, type of interleaving to distinguish from the prior art or memory art." A167 (D.I. 312, Ex. H). After the applicant submitted new claims

in a supplemental amendment (A168-171 (D.I. 312, Ex. H)), the examiner issued a notice of allowance following examiner's amendments. A176-180 (D.I. 312, Ex. H).

The only "distinct features" identified in the examiner's discussion of allowable subject matter were "specifying a maximum number of bytes available to be allocated to [an interleaver/deinterleaver] in a transmitted or received message, determining the amount of memory required by the [interleaver/deinterleaver], and then allocating the bytes of a shared memory to the [interleaver/deinterleaver] wherein the bytes allocated do not exceed the maximum number of available bytes specified in the message." A180 (D.I. 312, Ex. H) The examiner explained that "[t]he closest prior art, Fadavi-Ardekani et al (U.S. Pat. No. 6,707,822) discloses sharing a memory between the interleavers and deinterleavers of multiple ADSL sessions, fails to suggest limiting the memory allocated to the interleaver to a maximum number of bytes available that was specified in a transmitted or received message." *Id*. Thus, the only purportedly novel aspect of the claimed invention was the content of the message.

TQ Delta's summary of the Family 3 patents contains a number of inaccuracies and improper argument that ignores the intrinsic evidence. For example, TQ Delta incorrectly states that memory allocation involves "memory cells"—but the specification, claims, and prosecution history of the Family 3 patents never once mention "memory cells." Unsurprisingly, the diagrams of "memory cells" included at *supra* at pp. 14, 16, 17, and 19 of TQ Delta's Opening Brief are not supported by any citations to the intrinsic evidence—the concept of "memory cells" does not come from the intrinsic record. TQ Delta also purports to draw a distinction between allocated memory and used memory, arguing that "the interleaver or deinterleaver may actually use less memory than the amount of shared [memory] allocated to the function." *Supra* at p. 17. That assertion also finds no support in the intrinsic record.

IV. ASSERTED CLAIMS

For the convenience of the Court, the Asserted Claims of the Family 3 Patents are set forth below:

'890 Patent

5. A method of allocating shared memory in a transceiver comprising:

transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;

determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;

allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for reception at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;

allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate; and

deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver,

wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.

'381 Patent

5. A non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver comprising:

transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;

determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;

allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for reception at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;

allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate; and

deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.

'882 Patent

13. A system that allocates shared memory comprising:

a transceiver that performs:

transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;

determining an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;

allocating a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;

allocating a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes received at a second data rate; and

deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.

'048 Patent

1. A system that allocates shared memory comprising:

a transceiver that is capable of:

transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver;

determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory;

allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate,

wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message;

allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and

interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

’126 Patent

1. An apparatus comprising:

a multicarrier communications transceiver that is configured to perform a first interleaving function associated with a first latency path and perform a second interleaving function associated with a second latency path, the multi carrier communications transceiver being associated with a memory,

wherein the memory is allocated between the first interleaving function and the second interleaving function in accordance with a message received during an initialization of the transceiver and wherein at least a portion of the memory may be allocated to the first interleaving function or the second interleaving function at anyone particular time depending on the message.

10. An apparatus comprising:

a multicarrier communications transceiver that is configured to generate a message during an initialization of the transceiver, perform a first deinterleaving function associated with a first latency path, and perform a second deinterleaving function associated with a second latency path, the transceiver being associated with a memory,

wherein at least a portion of the memory may be allocated to the first deinterleaving function or the second deinterleaving function at anyone particular time and wherein the generated message indicates how the memory has been allocated between the first deinterleaving function and second deinterleaving function.

’473 Patent

19. An apparatus comprising:

a multicarrier communications transceiver that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path, the multi carrier communications transceiver being associated with a memory,

wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver and

wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at anyone particular time depending on the message.

28. An apparatus comprising:

a multicarrier communications transceiver that is configured to generate a message during an initialization of the transceiver, perform an interleaving function associated with a first latency path, and perform a deinterleaving function associated with a second latency path, the transceiver being associated with a memory,

wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at anyone particular time and wherein the generated message indicates how the memory has been allocated between the interleaving function and the deinterleaving function.

V. CLAIM TERMS WITH AGREED-TO CONSTRUCTIONS.

Set forth below is a claim term from the Asserted Claims of the Family 3 Patents for which the parties have agreed to a construction.

Claim Term	Agreed Construction
"multicarrier"	"having multiple carrier signals that are combined to produce a transmission signal"

VI. DISPUTED CLAIM TERMS.

A. "transceiver"

Plaintiff's Proposed Construction	Defendants' Proposed Construction
"communications device capable of transmitting and receiving data wherein the transmitter portion and receiver portion share at least some common circuitry"	*"communications device capable of transmitting and receiving data"*

1. Plaintiff's Opening Position

This Court has previously construed this term. *See* A112 (*TQ Delta, LLC v. Comcast Cable Communications, LLC*, 15-cv-00611-RGA, D.I. 214 (November 30, 2016), "Memorandum Opinion"). There the Court rejected the construction that Defendants urge here. *Id*. Plaintiff TQD proposes that the Court adopt the same construction that it adopted for the

term "transceiver" in TQD's MoCA cases,[3] namely "communications device capable of transmitting and receiving data wherein the transmitter portion and receiver portion share at least some common circuitry." *See, e.g.*, See A112 (Memorandum Opinion at p. 8, TQ Delta, LLC v. Comcast Cable Communications, LLC, No. 1:15-cv-00611-RGA, (D. Del. November 30, 2016), D.I. 214). With respect to Defendants' proposed construction, it is unreasonably broad and can be interpreted, incorrectly, to mean that that the transmitter and receiver are separate or isolated and are functionally wholly unrelated.

A "transceiver" is a well-understood term of art and under the generally accepted definition, a transceiver is capable of transmitting and receiving and the transmitting and receiving functions are implemented using at least some common circuitry. A91 (IEEE Standard Dictionary of Electrical and Electronics Terms, 4th ed. (1998) at p. 1028) (defining transceiver as "[t]he combination of radio transmitting and receiving equipment in a common housing, . . . , and employing common circuit components for both transmitting and receiving"); A78 (Hargrave's Communications Dictionary (2001) at p. 540); A96 (Merriam Webster's Collegiate Dictionary, 10th ed. (1993) at p. 1253) (defining transceiver as "a radio transmitter-receiver that uses many of the same components for both transmission and reception"); *see also* A692-A693 (Cooklev Decl. at ¶ 45). In accordance with this widely accepted definition of transceiver, the '890 patent specification similarly contemplates that the transmitter and receiver of the transceiver share components or circuitry. A3 ('890 Patent, Fig. 1) (shared processing module 110, shared memory 120, etc.) Also, because the transmitting entity and the receiving entity are

[3] *TQ Delta, LLC v. Comcast Cable Communications, LLC* (C.A. No. 15-cv-611-RGA), *TQ Delta, LLC v. Coxcomm LLC et al.* (C.A. No. 15-cv-612-RGA), *TQ Delta, LLC v. DirectTV, LLC* (C.A. No. 15-cv-613-RGA), *TQ Delta, LLC v. Dish Network Corp. et al.* (C.A. No. 15-cv-614-RGA-MPT), *TQ Delta, LLC v. Time Warner Cable, Inc. et al.* (C.A. No. 15-cv-615-RGA-MPT), *TQ Delta, LLC v. Verizon Services Corp.* (C.A. No. 15-cv-616-RGA-MPT) (collectively, "the MoCA cases").

part of a single device, they share some circuitry. A693 (Cooklev Decl.) at ¶ 46. For example, clock generation circuitry is typically shared. *Id.* Multicarrier transceivers, such as DSL transceivers, use portions of the same communication channel for transmitting and receiving and, thus, require some coordination between the transmitter and receiver. *Id.* Such coordination would be more difficult if the transmitting and receiving entities were completely separate. *Id.* Consistent with this widely-accepted definition of transceiver, the Family 3 Patents similarly contemplate a device capable of transmitting and receiving where the transmitter and receiver share at least some common circuitry.

In contrast, the broad definition of "transceiver" proposed by Defendants could incorrectly be interpreted to include those types of designs where the transmitter is isolated from, and functionally unrelated to, the receiver (e.g., communicating using an entirely different communication scheme over a different medium) – something not contemplated by the patents-in-suit and the extrinsic evidence. A693 (Cooklev Decl.) at ¶ 47.

Based on the foregoing, a person having ordinary skill in the art would have understood that a "transceiver" is a "communications device capable of transmitting and receiving data wherein the transmitter portion and receiver portion share at least some common circuitry."

2. Defendants' Answering Position

The parties agree that a "transceiver" is a "communications device capable of transmitting and receiving data," but TQ Delta's proposed construction adds an additional requirement (*i.e.*, the "wherein the transmitter portion and receiver portion share at least some common circuitry" clause), which is not supported by the intrinsic record.

Defendants' proposed construction is correct because the Family 3 specification recites that the claimed transceivers must be capable of both transmitting and receiving data—no more and no less. *See, e.g.*, A7 ('890 patent) at 4:41-65 ("The transceiver 100 includes a transmitter

portion 200 and a receiver portion 300…"); *see also, e.g.*, A35 ('882 patent) at claim 13 and A47 ('048 patent) at claim 1 ("A transceiver [that performs/is capable of] transmitting or receiving… a message during initialization…"). There is no requirement in the specification or the claims that the transmitter and receiver share circuitry. *See Phillips*, 415 F.3d at 1315 ("Claims must always be read in light of the specification [which] makes plain what the appellants did and did not invent ....") (*quoting In re Fout*, 675 F.2d 297, 300 (CCPA 1982)).

TQ Delta points to Figure 1 of the Family 3 specification as support for its proposed construction, but nothing in Figure 1 or elsewhere in the specification suggests that the transmitter portion 200 and the receiver portion 300 include common physical circuitry. Nowhere do the drawings or the specification indicate that the shared processing module 110 or the shared memory 120 are physical circuitry. *See* A725-A726 (Jacobsen Decl.) at ¶¶ 28-31. Indeed, the specification states that any modules may be implemented entirely in *software*. *See* A7 ('890 patent) at 3:50-53. Similarly, TQ Delta's expert contends elsewhere that shared memory 120 "need not be a 'single' physical object." A694 (Cooklev Decl.) at ¶ 50. As such, TQ Delta's construction is not supported by the intrinsic record and is undermined by its own expert's testimony.

TQ Delta also relies on extrinsic evidence (dictionary definitions and a conclusory expert declaration) in support of its proposed construction, but such evidence is "less reliable than the patent and its prosecution history in determining how to read claim terms." *Phillips*, 415 F.3d at 1318. TQ Delta's dictionary definitions are inapposite because they relate to radios, and the only other support TQ Delta relies upon is a conclusory expert declaration that actually contradicts its position.

As discussed in Defendants' responsive claim construction brief for the Family 1 patents,

the Court's previous construction of the term "transceiver" in another case involving different patents that are unrelated to the Family 3 patents and have a different specification should have no bearing here. *See e.Digital Corp. v. Futurewei Tech., Inc.*, 772 F.3d 723, 727 (Fed. Cir. 2014) ("a claim of an unrelated patent 'sheds no light on' the claims of the patent in suit").

Accordingly, the Court should construe "transceiver" as "communications device capable of transmitting and receiving data."

3. Plaintiff's Reply Position

Defendants' argument flips the claim construction process on its head by ignoring the ordinary meaning of the claim term and asserting that the specification does not define "transceiver" as Plaintiff proposes. But neither TQ Delta nor Defendants contend that the patent specification imparts a novel meaning to the term "transceiver." In referencing the specification, TQ Delta was merely pointing out that the specification is consistent with the ordinary meaning of "transceiver." Therefore, "the term [transceiver] takes on its ordinary meaning." *Optical Disc Corp. v. Del Mar Avionics*, 208 F.3d 1324, 1334 (Fed. Cir. 2000) (noting that "[w]ithout evidence in the patent specification of an express intent to impart a novel meaning to a claim term, the term takes on its ordinary meaning."); *see also Hoechst Celanese Corp. v. BP Chemicals Ltd.*, 78 F.3d 1575, 1578 (Fed. Cir. 1996) ("A technical term used in a patent document is interpreted as having the meaning that it would be given by persons experienced in the field of the invention, unless it is apparent from the patent and the prosecution history that the inventor used the term with a different meaning.").

Defendants do not dispute TQ Delta's contention that, because a "transceiver" is a well-understood term of art, it should be accorded its ordinary meaning. Defendants only complaint with TQ Delta's construction appears to be that the specification does not explicitly describe the shared circuitry of the transceiver. While this is not relevant given that TQ Delta's construction

is based on the plain meaning of the term "transceiver," it is also not true. As previously stated, the specification explains that the transmitter and receiver use the same "shared memory." In an attempt to explain this away, Defendants argue that "nowhere do the drawings or specification indicate that . . . the shared memory 120 are physical circuits" and that "TQ Delta's expert contends . . . that shared memory 120 'need not be a 'single' physical object.'" These arguments (whether true or not), again, miss the point. TQ Delta is not arguing that the plain meaning of transceiver should be limited by the specification; rather, TQ Delta is merely showing that the specification is consistent with that plain meaning. Defendants do not argue, much less prove, that the specification requires that shared memory 120 necessarily does not comprise physical circuits (Defendants do not even describe how such an implementation is possible) or that the shared memory 120 necessarily does not comprise one physical unit (in any event a shared memory space can comprise one or more physical units). Thus, the specification is consistent with TQ Delta's construction that clarifies that "the transmitter portion and receiver portion share at least some common circuitry."

Defendants complain about the use of dictionary definitions, which this Court previously relied on and which confirm TQ Delta's proposed construction. But there is nothing improper about such reliance. *Optical Disc Corp. v. Del Mar Avionics*, 208 F.3d 1324, 1334 (Fed. Cir. 2000) (noting that "extrinsic evidence may be considered if needed to assist in determining the meaning or scope of technical terms in the claims."). It is well established that a court may rely on dictionary definitions when construing technical claim terms, even though such dictionaries are extrinsic evidence. *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1584 n. 6 (Fed. Cir. 1996) (noting that "[a]lthough technical treatises and dictionaries fall within the category of extrinsic evidence, as they do not form a part of an integrated patent document, they are worthy

of special note" and that "Judges are free to consult such resources at any time in order to better understand the underlying technology and may also rely on dictionary definitions when construing claim terms, so long as the dictionary definition does not contradict any definition found in or ascertained by a reading of the patent documents."); *see also Vanguard Prod. Corp. v. Parker Hannifin Corp.*, 234 F.3d 1370, 1372 (Fed. Cir. 2000) (noting that "a dictionary is often useful to aid the court in determining the correct meaning to be ascribed to a term as it was used.").

Defendants attempt to distinguish TQ Delta's dictionary definitions by insinuating that the use of the word "radio" in the definitions means that those dictionary definitions are inapplicable to the recited "transceiver" of the Family 3 Patents. Without saying as much, Defendants seek to draw a distinction between wireless and wired transceivers. However, Defendants fail to recognize that the claimed inventions are "described in relation to sharing resources in a wired and/or wireless communications environment." A7 ('890 patent) at 3:6-8; A10 ('890 patent) at 9:38-39. (stating that "the above-described system can be implemented on wired and/or wireless telecommunications devices"); *see also* A750 (Cooklev Reply Decl.) at ¶ 12. Thus, the "transceiver" recited in the claims has a meaning that is no different than the meaning ascribed to transceiver by the cited dictionary definitions.

Separately, Defendants recognize that this Court previously construed the term "transceiver" in another group of cases [– the MoCA cases –] involving TQ Delta. Defendants attempt to distinguish the claim construction in the MoCA cases by pointing out that the patent specifications at issue there are different than the Family 3 specification. But the Court's construction in the MoCA cases did not rely on anything unique about the specifications there. Rather, the Court reasoned that although some of the patents "*do not provide any specific*

indication that any circuitry is shared between the two," "[e]valuating the intrinsic evidence in light of [the] dictionary definitions suggests that the transmitter and receiver portions do share common circuitry or components." *See* A113 (Memorandum Opinion at p. 9, *TQ Delta, LLC v. Comcast Cable Communications, LLC*, No. 1:15-cv-00611-RGA, (D. Del. November 30, 2016), D.I. 214) (emphasis added). The Court then went on to "construe transceiver to mean 'a communications device capable of transmitting and receiving data wherein the transmitter portion and receiver portion share at least some common circuitry.'" Nothing in the Defendants' argument undermines the Court reasoning in the MoCA cases.

4. Defendants' Sur-reply Position

TQ Delta has not shown why the Court should add an extraneous and immaterial limitation to the term "transceiver" (and by extension, to every asserted claim). Defendants' construction reflects what the claims and the intrinsic record require of the term, is consistent with the understanding of a person of ordinary skill in the art, and should be adopted.

In the Family 3 patents, the intrinsic evidence – the specification and the claims – requires only that a transceiver be able to transmit and receive. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1315 (Fed. Cir. 2005) ("[C]laims 'must be read in view of the specification, of which they are a part" and "the specification 'is always highly relevant to the claim construction analysis.'") (citations omitted). Nothing in the intrinsic record requires that the claimed transmitter and receiver portions must also share some common circuitry. *See, e.g.*, A7 ('890 patent), col. 3:61-67; *see also* A3 (Fig. 1). Defendants' construction is consistent with that understanding.

TQ Delta's proposed requirement for "common circuitry" would render the claims' requirement for a shared memory redundant. The sole intrinsic evidence TQ Delta points to in its Reply are the specification's references to "shared memory," and it identifies no other basis in

the intrinsic record for common circuity. *Supra* at p. 30. The claims themselves recite the concept of "shared memory," and thus describe the degree to which any circuitry must be shared. If a transceiver itself required "common circuitry," it would be redundant to specify elsewhere in the claim that memory must be "shared."

TQ Delta argues that it is not trying to limit the meaning of "transceiver" to any usage in the specification, but is merely showing that such usage is "consistent" with "plain meaning." *Supra* at p.30. But even TQ Delta's implausible explanation for trying to limit the meaning of "transceiver" fails if they have the incorrect "plain meaning." TQ Delta's purported "plain meaning" is drawn entirely from extrinsic evidence in the form of dictionary definitions and a conclusory expert declaration. As noted previously by Defendants, TQ Delta's dictionary definitions describe a "radio transmitter-receiver," which is not at issue here. *See* A96 (general purpose dictionary defining "transceiver" as a "radio transmitter – receiver"); A91 ("the combination of radio transmitting and receiving equipment . . ."). Moreover, TQ Delta's reliance on carefully selected dictionary definitions is misplaced, as other dictionaries from the time of the alleged invention do not require "common circuitry," and state only that a transceiver is "any device that transmits and receives," or "a device that can both transmit and receive signals on a communication medium." A632 (Newton's Telecom Dictionary, 2004), at p. 846; A635 (Oxford Dictionary of Computing, 2004), at p. 542.

The cases TQ Delta cites for its heavy reliance on extrinsic evidence *all* pre-date *Phillips*. *See Phillips*, 415 F.3d at 1319 ("[E]xtrinsic evidence may be useful to the court, but it is unlikely to result in a reliable interpretation of patent claim scope unless considered in the context of the

intrinsic evidence."). Moreover, TQ Delta's own cited authority confirms that dictionary definitions have a limited role in claim construction.[4]

Plaintiff's reliance on the Court's prior ruling in the MoCA litigation fares no better here than it did in Plaintiff's opening brief. When the Court previously construed this term, the *only* intrinsic evidence that suggested a need for "common circuitry" was found in U.S. Patent No. 8,611,404, which is ***unrelated*** to Family 3 and ***is not asserted here***. There, the Court found that:

> These patents do not provide any specific indication that any circuitry is shared between the two. In the low power mode patents, however, the specification and figure do indicate the presence of shared components. For example, the clock, controller, and frame counter are shared by the transmitter and receiver portions of the transceiver. ('404 patent at Fig. 1).

TQ Delta, LLC v. Comcast Cable Corp., C.A. No. 1:15-cv-00611-RGA, 2016 WL 7013481, at *4 (D. Del. Nov. 30, 2016). TQ Delta has not identified any evidence intrinsic to these patents that supports its requirement for common circuitry in ***the Family 3 patents***, which were not at issue in the MoCA litigation. TQ Delta's reliance on intrinsic evidence from unrelated patents has no basis in the law, and should be rejected.

Accordingly, "transceiver" should be construed as "communications device capable of transmitting and receiving data."

[4] Each of the decisions relied upon by TQ Delta are distinguishable. The Federal Circuit in *Optical Disc Corp. v. Del Mar Avionics*, 208 F.3d 1324, 1334 (Fed. Cir. 2000) first noted that "[u]sually, an analysis of the intrinsic evidence alone will resolve any ambiguity in a disputed claim term," before construing the claims in view of the specification and some dictionary definitions. In *Vanguard Prods. Corp. v. Parker Hannifin Corp*., 234 F.3d 1370, 1372 (Fed. Cir. 2000), the Federal Circuit found that it was proper to rely on dictionary definitions, though they "may not enlarge the scope of a term." Here, by contrast, TQ Delta seeks to introduce an additional limitation that is not supported by the intrinsic record into its construction. Finally, in *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582-83 (Fed. Cir. 1996), the Federal Circuit noted the importance of looking at the claims, the specification, and the prosecution history, and criticized the district court for relying on dictionary definitions.

B. "shared memory"

Plaintiff's Proposed Construction	Defendants' Proposed Construction
"a common memory space used by at least two functions, where particular memory cells within the common memory space can be used by either one of the functions"	*"single common memory in a transceiver used by at least two functions corresponding to at least two latency paths"*

1. Plaintiff's Opening Position

The parties agree that shared memory is "common memory" "used by at least two functions." However, Defendants urge that common memory be qualified as "single." A694 (Cooklev Decl.) at ¶ 50. As an initial matter, "single common memory" is vague. For example, it is unclear if "single" implies shared memory that is in a single semiconductor chip, a single memory module, or a single group of memory modules. *Id*. Thus, Defendants' qualification of common memory with the "single" modifier is unhelpful. In any event, the specification does not limit the claimed shared memory to a single semiconductor chip or single memory module, as Defendants urge. And although, the embodiment set forth in Fig. 1 depicts shared memory 120 as a single block, the specification does not limit the scope of shared memory to a "single" common memory, whatever that might mean. A3 ('890 Patent) at Fig. 1; A694 (Cooklev Decl.) at ¶ 50. Therefore, Defendants' attempt to limit the scope of shared memory to a "*single* common memory" is improper and should be rejected. *See Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004) (noting that "[e]ven when the specification describes only a single embodiment, the claims of the patent will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using 'words or expressions of manifest exclusion or restriction.'") (citations omitted).

The parties agree that the shared memory "is used by at least two functions" and is "common" with respect to those functions. However, without the clarification provided by TQ

Delta's construction, namely, "where particular memory cells within the common memory space can be used by either one of the functions," Defendants' construction may be applied in an incorrectly overly broad manner. A694 (Cooklev Decl.) at ¶ 50. Specifically, Defendants' construction would include devices where a first function is restricted at all times to only using a first portion of a memory (e.g., a memory module) and a second function is restricted at all times to only using a second portion of the same memory. A694 (Cooklev Decl.) at ¶ 50. In such an arrangement, where portions of the same memory are dedicated at all times to one function or the other, the memory is neither common to, nor shared by, the two functions. *Id*. TQ Delta's construction, on the other hand, properly clarifies that a shared memory is one that allows particular memory cells to be used by either one of the two functions. A694 (Cooklev Decl.) at ¶ 49.

Defendants' construction is further problematic because it may be interpreted to required that two functions both use the same particular memory cell of a memory at the same time – an interpretation that would be inconsistent with the Family 3 Patents. Interleaving and deinterleaving are two separate functions, with interleaving being performed by the transmitter section of the transceiver and deinterleaving being performed by the receiver section of the transceiver. A688-A689 (Cooklev Decl.) at ¶ 38. Moreover, interleaving operates to interleave a set of codewords that are ready to be transmitted, while deinterleaving operates to deinterleave a different set of codewords that has been received. Thus, the interleaving and deinterleaving operations use separate memory cells of shared memory. *Id*. TQ Delta's construction also accounts for this by providing that "particular memory cells within the common memory space can be used by either one of the functions."

Finally, Defendants seek to read into "shared memory" a requirement that the two functions "correspond[] to at least two latency paths." While this accurately describes the manner in which the shared memory is used in the context of explicit recitations in some claims of the Family 3 Patents, it is not a requirement embodied in the words "shared memory." Thus, Defendants' construction is an attempt to rewrite the claim and is improper. *See Embrex, Inc. v. Serv. Eng'g Corp.*, 216 F.3d 1343, 1348 (Fed. Cir. 2000) (noting that claim construction is simply a way of elaborating the normally terse claim language in order to understand and explain, but not to change, the scope of the claims).

For the reasons set forth above the Court should adopt TQ Delta's construction.

2. Defendants' Answering Position

The primary disputes for this term are whether the memory that is shared is a *single* common memory, and whether the two functions used by the memory correspond to multiple latency paths. Defendants' proposed construction correctly reflects that the invention requires a single common memory that is allocated and shared, whereas TQ Delta's proposed construction introduces ambiguity and confusion by substituting the vague term "common memory space" for the term "shared memory." "Common memory space" is not a commonly used term. A person of ordinary skill would not have known whether "a common memory space" refers to hardware (physical memory addresses) or software (a collection of addresses corresponding to and identifying physical storage locations but abstracted from the physical memory implementation.) *See* A728-A729 (Jacobsen Decl.) at ¶ 38.

Defendants' proposed construction properly reflects that the shared memory is "in a transceiver," a point that TQ Delta does not dispute in its brief and that its expert acknowledges. *See* A684 (Cooklev Decl.) at ¶ 28 ("An interleaver is a component *in a transceiver* . . . .")

(emphasis added); *id.* at ¶ 29 ("An important element of the interleaver is the interleaver memory that is used to perform the interleaving.").

Defendants' proposal also reflects the purpose of the alleged invention and is supported by the intrinsic evidence. *See Phillips*, 415 F.3d at 1316 ("The construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction.") (citation omitted). The first sentence of the Abstract indicates that the purpose of the alleged invention is to "share memory… amongst a plurality of transmitter and/or receiver latency paths." *See* A1 ('890 patent) at Abstract; *see Lucent Techs. Inc. v. Gateway, Inc.*, 525 F.3d 1200, 1207-08 (Fed. Cir. 2008) (overturning district court's construction where it was not supported by the abstract and summary of invention); *NEC Corp. v. Hyundai Elecs. Indus. Co.*, 30 F. Supp. 2d 546, 553 (E.D. Va. 1998) ("the purpose of the invention may guide claim construction since 'the problem the inventor was attempting to solve, as discerned from the specification and prosecution history, is a relevant consideration' in construing claims") (citation omitted).

The claim language itself supports the portion of Defendants' construction requiring a "single common memory." Each of the asserted claims in which this term appears refers only to "a" or "the" shared memory, strongly suggesting one single memory. *See* A11 ('890 patent) at claim 5; A23 ('381 patent) at claim 5; A35 ('882 patent) at claim 13; A47 ('048 patent) at claim 1. This understanding is also consistent with how one of ordinary skill in the art would interpret this claim language. *See* A728 (Jacobsen Decl.) at ¶ 36.

The specification further confirms that shared memory is a single common memory in a transceiver. The specification provides a number of examples describing "one memory space" of a certain number of Kbytes. *See* A8 ('890 patent) at 6:59-60 (describing "three latency paths that

share one memory space containing at least (16+4)=20 Kbytes"); A9 ('890 patent) at 7:21-22 ("the three latency path share one memory space containing a least 3*4=12 Kbytes"). Moreover, the claims and the specification repeatedly discuss "allocating" or "allocation" of shared memory. The use of the term "allocating" strongly suggests the division of a single common memory.

The Family 3 Patents claim priority to a provisional application filed on October 12, 2004. A 2004 Dictionary of Computing definition for the term "shared memory" is: "[t]he use of the ***same portion of memory*** by two distinct processes, or the memory so shared. Shared memory is used for interprocess communication and for purposes, such as common subroutines, that lead to compactness of memory." A556 (2004 Oxford University Press Dictionary of Computing, p480). Further, one of ordinary skill in the art would understand "shared memory" to refer to a single common memory. *See* A728-A729 (Jacobsen Decl.) at ¶ 38.

TQ Delta attempts to manufacture ambiguity where there is none to dispute Defendants' construction. First, TQ Delta asserts that it is "unclear if 'single' implies shared memory that is in a single semiconductor chip, a single memory module, or a single group of memory modules." *Supra* at p. 35. But this assertion is not rooted in any alternate potential meanings in the specification, which does not contain any references to "chips" or "memory modules." Second, TQ Delta argues that Defendants' construction would include devices where a first function is restricted at all times to a first portion of memory, and a second function is restricted at all times to using a second portion of memory. *Id*. at p. 36. But Defendants' construction explicitly states that the single common memory is "used by"—and thus, shared by— at least two functions, and nothing in the construction suggests the "restricted at all times" limitation that TQ Delta imagines. *See* A10-11 ('890 patent) at claims 1 and 5, A23 ('381 patent) at claim 5, A35 ('882

patent) at claim 13, A47 ('048 patent) at claim 1; *see also* A729-A730 (Jacobsen Decl.) at ¶ 39. Finally, and contrary to its argument that Defendants' construction restricts a given function to a given portion of memory at all times, TQ Delta argues that Defendants' construction "may be interpreted to require[ ] that two functions both use the same particular memory cell of a memory at the same time." *Supra* at p. 36. But Defendants' construction has nothing to do with "memory cells," which, as discussed above, is a concept lacking any basis in the specification or the claims.

TQ Delta's expert incorrectly asserts, without citing any intrinsic or extrinsic evidence, that shared memory could be "multiple separate and discrete blocks of memory." A694 (Cooklev Decl.) ¶ 50. TQ Delta's proposal of "a common memory space" would thus allow memory to be split into configurations of memory that are not actually shared, for example, having one memory for the interleaver, and a different memory for the deinterleaver. *See* A728-A729 (Jacobsen Decl.) at ¶¶ 37-38. This is inconsistent with the alleged invention's purpose of sharing memory, is not supported by any intrinsic evidence, and should not be adopted.[5]

The portion of Defendants' proposed construction requiring that the two functions using the single common memory correspond to at least two latency paths is consistent with the purpose of the alleged invention to "share memory… amongst… latency paths," and is supported by other intrinsic evidence. *See* A1 ('890 patent) at Abstract; *see also, e.g.,* A7 ('890 patent) at 4:1-5 ("memory… can be shared among a plurality of transmitter and/or receiver latency paths, in a communications transceiver."), *id.* at 4:6-9 ("[T]he transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory and the shared memory can be

[5] TQ Delta's reliance on *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F3d. 898, 906 (Fed. Cir. 2004) is misplaced. Defendants' proposal does not restrict "shared memory" to a "single embodiment" but rather interprets "shared" according to the purpose of the alleged invention.

allocated to the interleaver and/or deinterleaver of each latency path."), A8 ('890 patent) at 6:57-64 (three latency paths that share one memory space"), A9 ('890 patent) at 7:7-25 ("the three latency path[s] share one memory space").

TQ Delta concedes that the use of latency paths "accurately describes the manner in which the shared memory is used in the explicit recitations" of the asserted claims. *Supra* at p. 37. Yet TQ Delta improperly attempts to rewrite the claims by cutting out this admitted context. *See Phillips*, 415 F.3d at 1314 ("the claims themselves provide substantial guidance as to the meaning of particular claim terms"); *Interactive Gift Express, Inc. v. Compuserve Inc.*, 256 F.3d 1323, 1331 (Fed. Cir. 2001) ("the analytical focus must begin and remain centered on the language of the claims themselves").

TQ Delta's proposed construction should be rejected. TQ Delta's proposed construction introduces the concept of "particular memory cells" from left field. "Memory cells" are not discussed or defined anywhere in the intrinsic evidence. That is why TQ Delta's Opening Claim Construction brief has no citations to the intrinsic record in support of its discussion or figures representing "memory cells." Moreover, in the context of the Family 3 patents, which present the alleged invention for DSL, a person having ordinary skill in the art would have simply referred to memory in terms of numbers of bytes. *See* A723-A725, A730 (Jacobsen Decl.) at ¶¶ 24-25, 40.

The Court should construe "shared memory" as "single common memory in a transceiver used by at least two functions corresponding to at least two latency paths."

3. Plaintiff's Reply Position

Defendants argue that "[e]ach of the asserted claims in which this term appears refers only to 'a' or 'the' shared memory, strongly suggesting one single memory." *See supra* at p. 38. However, "a" means one or more not one as Defendants contend. *Baldwin Graphic Sys., Inc. v.*

Siebert, Inc., 512 F.3d 1338, 1342 (Fed. Cir. 2008) (recognizing that "'a' or 'an' can mean 'one or more' is best described as a rule, rather than merely as a presumption or even a convention."); *SanDisk Corp. v. Kingston Tech. Co. Inc.*, 695 F.3d 1348, 1360 (Fed. Cir. 2012) (recognizing the general rule that the use of the indefinite articles "a" or "an" means "one or more."). "The exceptions to this rule are extremely limited: a patentee must 'evince a clear intent' to limit 'a' or 'an' to 'one.'" *Baldwin Graphic Sys., Inc.*, 512 F.3d at 1342 (quoting *KCJ Corp. v. Kinetic Concepts, Inc.*, 223 F.3d 1351, 1356 (Fed.Cir.2000)). Defendants' contention that the Family 3 Patents "strongly suggest[] a single memory" is not the type of statement that evidences "a clear intent to limit 'a'" to one or single.

Further, as explained by Dr. Cooklev, in the context of the specifications, "a" or "the" does not mean single. A751 (Cooklev Reply Decl.) at ¶14. Defendants attempt to shift the burden to TQ Delta to demonstrate why "a shared memory" should not be restricted to "one" or "single" is improper. Defendants seek the exception; but they have not proffered convincing evidence to support it. The Court should not make an exception to the general rule and should reject Defendants' attempt to restrict shared memory to "single."

With respect to TQ Delta's proposal that shared memory in relevant part means "common memory space" Defendants argue that "common memory space" is not a commonly used term. Even if true, "patent law allows the inventor to be his own lexicographer." *Autogiro Co. of Am. v. United States*, 384 F.2d 391, 397 (Ct. Cl. 1967). The Family 3 specification uses exactly this term, stating that "since the transmitter latency paths may share a common memory space . . . ." A9 ('890 Patent) at 8:2-5. Dr. Cooklev explains that "[t]he Family 3 Patent specifically refers to this physical shared memory as a common memory space." A751 (Cooklev Reply Decl.) at ¶ 15 (citing A9 ('890 Patent) at 8:3-4). Thus, TQ Delta's construction that

shared memory, in relevant part, is "a common memory space" is supported by the intrinsic record.

With respect to the remainder of the TQ Delta's construction, which states "where particular memory cells within the common memory space can be used by either one of the functions," Defendants complain that "memory cells" are not disclosed in the patent. Defendants' complaint is without merit. Dr. Cooklev explained that a person of ordinary skill in the art would understand that a memory cell is the smallest physical unit of memory. A_ (Cooklev Reply Decl.) at ¶ 6. With respect to Defendants' contention that "a person having ordinary skill in the art would have simply referred to memory in terms of numbers of bytes," Dr. Cooklev explained that although based on specific implementation, a byte may be the smallest addressable unit of memory, the byte in memory is nevertheless comprised of memory cells, typically 8 memory cells. *Id*. In any event, Defendants' expert, Dr. Jacobsen, recognizes that shared memory is comprised of physical memory locations. *See* A739-A740 (Jacobsen Decl.) at ¶¶ 60-61. Defendants' construction however does not account for this physical attribute of shared memory. It is noteworthy that, although elsewhere Defendants complain that "[a] person of ordinary skill would not have known whether 'a common memory space' refers to hardware (physical memory addresses) or software (a collection of addresses corresponding to and identifying physical storage locations but abstracted from the physical memory implementation.)," here Defendants resist TQ Delta's attempt to clarify that common memory space refers to hardware (particular memory cells). *See* A728-A729 (Jacobsen Decl.) at ¶ 38 ("TQ Delta's proposal introduces confusion in the construction of the term "shared memory" because it is unclear whether a "common memory space" refers to software or hardware.") Defendants cannot have it both ways.

Separately, Defendants and their expert agree that in the context of the Family 3 Patents, the interleaver and deinterleaver do not use the same physical locations of the shared memory at the same time. *See* A753 (Cooklev Reply Decl.) at ¶ 20 (citing A739 (Jacobsen Decl.) at ¶ 60). Further, Defendants recognize that a set of bytes within the shared memory may be allocated for use by only one of the two functions (interleaver or deinterleaver) at any one particular time. *See* A753 (Cooklev Reply Decl.) at ¶ 21 (citing A739-A740 (Jacobsen Decl.) at ¶ 61). Thus, there is no dispute that that in the context of the Family 3 Patents "the interleaver and deinterleaver exclusively use their respective allocations of common memory." *See* A753 (Cooklev Reply Decl.) at ¶ 19. However, Defendants construction does not account for this type of memory sharing. To the contrary, Defendants cite to a definition of shared memory found at A556. This definition provides that shared memory is the "use of the same portion of memory by two distinct processes, or memory so shared."[6] However, this definition is incomplete and ambiguous because it does not account for the parties' understanding that sharing memory is the concurrent yet exclusive use by the interleaver and deinterleaver of their respective memory allocations. *See* A752-A753 (Cooklev Reply Decl.) at ¶ 18 and A739 (Jacobsen Decl.) at ¶¶ 60-61. The portion of TQ Delta's construction that provides that "particular memory cells within the common memory space can be used by either one of the functions" accounts for the parties understanding of what shared memory means in the context of the patents.

With respect to Defendants construction, "two functions correspond[] to at least two latency paths" does nothing to define or describe shared memory but instead defines attributes of

[6] The second part of the definition that refers to the use of shared memory for interprocess communication, conflicts with the Family 3 Patents usage of shared memory and Dr. Jacobsen's understanding of shared memory at (A739-A740) ¶¶ 60-61. A753 (Cooklev Reply Decl.) at ¶ 19. Although, use of memory for interprocess communication is another type of memory sharing, it is not the type of memory sharing contemplated by the Family 3 Patents. *Id*.

the two functions. In fact, Defendants admit as much when they state that "[t]he portion of Defendants' proposed construction requiring that the two functions using the single common memory correspond to at least two latency paths is consistent with the purpose of the alleged invention to "share memory… amongst… latency paths." *See supra* at p._. This shows that Defendants' construction is incorrect because "claim construction is a function of the words of the claim not the 'purpose' of the invention[.]" *See Source Vagabond Systems Ltd. v. Hydrapak, Inc.*, 753 F.3d 1291, 1301 (Fed. Cir. 2014). The Court should reject Defendants' attempt to imbue "shared memory" with the purpose of the invention.

The Court should adopt TQ Delta's construction for shared memory because it accurately defines the disclosed shared memory.

4. Defendants' Sur-reply Position

There are three disputes between the parties with respect to this term. ***First***, TQ Delta's proposed construction improperly tries to broaden the scope of the claim by characterizing the claimed shared memory as a "common memory *space*." (emphasis added). Defendants submit that this should be rejected as unsupported by the record. ***Second***, TQ Delta's proposed construction introduces a concept of "particular memory cells" that is nowhere discussed in the intrinsic evidence, is supported only by TQ Delta's expert declaration, and is confusing. This also should be rejected. ***Third***, TQ Delta disagrees with the portion of Defendants' proposed construction linking shared memory to at least two latency paths. This portion of Defendants' proposed construction is rooted in the intrinsic evidence and should be part of the Court's construction for the "shared memory" term. We address each of these subsidiary disputes separately below.

(a) The Claimed "Shared Memory" Is a "Single Common Memory"

The intrinsic evidence establishes that shared memory is a single common memory in a transceiver, and that construction is consistent with the understanding of a person of ordinary skill in the art. *Supra* at pp. 38-39. The first two examples in the specification state that latency paths "share ***one*** memory space," that is, a single shared (or common) memory, containing at least a certain number of bytes, as opposed to TQ Delta's broader term, a "common memory space." *Id*. (emphasis added). The figure showing the claimed transceiver depicts a single common memory as well. A3 ('890 patent), Fig. 1. Defendants' proposed construction is correct in view of the intrinsic evidence.

TQ Delta focuses on the third and final example in the specification, which states that latency paths "share a common memory space" to argue that, rather than being simply another articulation of the "one," or single, memory space recited in the other examples, the term "common memory space" somehow implies that there may be multiple, separate memories. But the portion of the specification TQ Delta relies upon contains ***no definition*** of "common memory space" whatsoever. It states only that latency paths can share a single common memory space, and that information may be exchanged so that transceiver can choose a configuration. *See* A9 ('890 patent), col. 8:2-5 ("[S]ince the transmitter latency paths may share a common memory space[,] the first modem must know the total shared memory for all transmitter latency paths."). This single reference to a common memory space, without reference to a "shared memory," falls far short of clearly setting forth a definition of a term. *See Thorner v. Sony Comput. Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012) ("To act as its own lexicographer, a patentee must clearly set forth a definition of the disputed claim term other than its plain and ordinary meaning.") (citation omitted).

Indeed, viewed in the context of TQ Delta's construction as a whole, TQ Delta effectively contends that "common memory space" means the opposite of its plain and ordinary meaning. First, TQ Delta contends that the "shared memory" could be two (or more) physically separate memories. *Supra* at p. 42. Second, TQ Delta states that under its construction, one such separate memory could be allocated "exclusively" to one function, and a second separate memory "exclusively" to another function. *Id*. at pp. 43-45. There is no intrinsic evidence to support the contention that the patentee defined a "shared" or "common" memory to mean two physically separate memories each allocated exclusively to the other. TQ Delta would turn the plain meaning of "common" or "shared" on its head.

The way that the term "shared memory" is used in the claims and the specification – as "a" or "the" shared memory – supports Defendants' construction. The Federal Circuit has explained that the *Baldwin* case TQ Delta cites "does *not* set a hard and fast rule that 'a' always means one or more than one." *Harari v. Lee*, 656 F.3d 1331, 1341 (Fed. Cir. 2011) (emphasis added). Instead, the limitation must be read "in light of the claim and specification to discern its meaning," such that "[w]hen the claim language and specification indicate that 'a' means one and only one, it is appropriate to construe it as such even in the context of an open-ended 'comprising' claim." *Id*. (*citing Insituform Techs., Inc. v. Cat Contracting, Inc*., 99 F.3d 1098, 1105–06 (Fed. Cir. 1996) (analyzing the "claims, specification and file history" to determine that "a vacuum cup" means one and only one vacuum cup)). Thus, Defendants are not "shift[ing]" any "burden" onto TQ Delta by pointing out what the intrinsic evidence discloses. *See supra* at p. 42.

Baldwin itself explicitly considered whether construing "a" as "one or more" was consistent with the specification. *See Baldwin Graphic Sys., Inc. v. Siebert, Inc*., 512 F.3d 1338,

1343 (Fed. Cir. 2008) (explaining that multiple fabric rolls could still be "in intimate contact" with plastic sleeve, consistent with specification). The other cases TQ Delta relies upon in this regard are also inapposite. *See SanDisk Corp. v. Kingston Tech. Co.*, 695 F.3d 1348, 1360-61 (Fed. Cir. 2012) (construing "at least a user data portion and an overhead portion" as covering "one or more" such portions in part because "[t]he phrase 'at least' suggests that the claim covers more than one user data portion and overhead portion," and also finding that doctrine of claim differentiation also supported this construction because dependent claims recited "only one user data portion and only one overhead portion."); *KCJ Corp. v. Kinetic Concepts, Inc.*, 223 F.3d 1351, 1357 (Fed. Cir. 2000) (finding nothing in intrinsic evidence that would support construing "a… continuous… chamber" as one chamber).

(b) "Memory Cells" Is Unsupported By Anything In The Intrinsic Evidence And Is Confusing and Unnecessary.

Importing the term "particular memory cells" into the construction of "shared memory" would introduce needless ambiguity. TQ Delta relies entirely on the declaration of its expert to devise a meaning for this term, and for requiring a reference to hardware (i.e., particular memory cells) in its definition. While Defendants agree that "shared memory" must have some physical implementation in hardware, a person of ordinary skill in the art would not understand the phrase "shared memory," or even "common memory space," to require identification of specific hardware in the claim or the proposed construction. A759-A760 (Jacobsen Reply Decl.), ¶¶ 3-4.

Here, TQ Delta's addition of "particular memory cells" has no basis in the intrinsic evidence. Regardless of whether "memory cells" are instantiated in hardware, the Family 3 patents provide no reason to introduce such purely extrinsic terminology into any of the claims. *Supra* at pp. 21-22, 40-41. Contrary to TQ Delta's assertions, there is no support in the intrinsic record for suggesting that the amount of memory used can be less than the amount of memory

allocated to each function. *Id*. at pp. 21-22. To the extent TQ Delta's references to any shared "understanding" by the parties (*id* at pp. 44-45) is intended to refer to such a distinction, Defendants do not share any such "understanding." As explained in Defendants' Response, the 2004 Dictionary of Computing definition of "shared memory" is consistent with the usage of that term in the claims, and the understanding of a person of ordinary skill in the art. *See id*. at p. 39.

(c) "Shared Memory" Is Used By At Least Two Functions.

TQ Delta criticizes Defendants' definition for including the concept that the shared memory is used by at least two functions corresponding to at least two latency paths. TQ Delta states that both parties agree that the interleaver and deinterleaver functions do not use the same portions of memory at the same time. This may be so, but that concept appears nowhere in TQ Delta's proposed construction and is further evidence of TQ Delta's attempt to broaden the claims with its proposed construction. Under TQ Delta's proposed definition, the "shared memory" could be any number of separate memory modules, where "particular memory cells . . . ***can*** be," but need not be, used by more than one function. Taken to its logical conclusion, Plaintiff's definition could read on separate memory modules where none of the memory is actually used by or allocated to more than one function. This effectively removes any requirement that the memory is "shared" by more than one function, and the Court should adopt Defendants' construction.

TQ Delta's reliance on *Source Vagabond Systems* for the proposition that considering the purpose of the claimed invention as a whole is improper does not save its construction. In that case, the plaintiff invoked the alleged "purpose" to justify "adding words to otherwise unambiguous claim language" and recapturing claim scope explicitly disclaimed during prosecution. *Source Vagabond Sys. Ltd. v. Hydrapak, Inc*., 753 F.3d 1291, 1299-1301 (Fed. Cir. 2014) (affirming sanctions where plaintiff made "frivolous" argument that "the slot being

narrower than the diameter of the rod, so that the sealer is only to be slidingly mounted sideways over the rod" should be construed as "the slot is narrower than the diameter of the rod ***together with the container folder over it***, so that the sealer is only to be slidingly mounted sideways over the rod ***and the container***") (emphasis added). Here, sharing memory among two latency paths is not just a purpose of the invention as a whole, but is the purpose evident from the context of the claims themselves, when viewed in light of the specification. *Supra* at pp. 40-41. TQ Delta also fails to address the cases cited in Defendants' Response, which confirm that courts properly take disclosures in an Abstract into account when construing claim terms. *See id*. at p. 38.

C. "amount of memory"

Plaintiff's Proposed Construction	Defendants' Proposed Construction
plain meaning or "number of units of memory"	*"number of bytes of memory"*

1. Plaintiff's Opening Position

TQ Delta submits that this claim term requires no construction because the plain meaning of the words "amount of memory" requires no further clarification for the factfinder. "[C]laim construction is a matter of resolution of disputed meanings and technical scope, to clarify and when necessary to explain what the patentee covered by the claims, for use in the determination of infringement." *O2 Micro Int'l Ltd.*, 521 F.3d at 1362 (citing *U.S. Surgical Corp. v. Ethicon, Inc.*, 103 F.3d 1554, 1568 (Fed.Cir.1997)). No such clarification or explanation is necessary here.

To the extent the Court believes that it is necessary to construe "amount of memory," the parties are in agreement that this term indicates a quantity of memory. The parties proposed constructions diverge, however, in that Defendants' construction adds the requirement that the

quantity be specified in "bytes." But the claim language does not recite any particular units for the quantity. For this reason, Defendants' construction is arbitrary and unduly narrow.

The term "byte" refers to a grouping of "bits"; for example, it is often used to refer to a group of eight bits. While a "byte" is one unit by which an amount of memory can be specified, there is no reason why an "amount of memory" cannot be specified in different units. For example, memory could be specified in bits, or kilobytes, or any other unit that indicates the quantity of memory. *See, e.g.*, A136 (IEEE Standard Dictionary of Electrical and Electronics Terms, 4th ed. (1988) at 96) (defining bit as a "unit of storage capacity"). A byte is merely one measure of memory.

In contrast to Defendants' overly narrowly construction, TQ Delta's proposed construction accounts for the different measures of memory. To the extent the Court believes that the term requires construction, the Court should adopt TQ Delta's construction and reject Defendants' construction.

2. Defendants' Answering Position

Defendants' proposed construction correctly reflects that (1) there is a dispute regarding the scope of this term, and (2) that an amount of memory is measured in terms of bytes, and not some other undefined "units." Regarding the first point, the term should be construed because a plain meaning construction would not "resolve a dispute about claim scope that has been raised by the parties." *Eon Corp. IP Holdings v. Silver Spring Networks*, 815 F.3d 1314, 1319 (Fed. Cir. 2016) ("By determining only that the [disputed] terms should be given their plain and ordinary meaning, the [district] court left this question of claim scope unanswered, leaving it for the jury to decide. This was legal error.").

Regarding the second point, Defendants' proposed construction is supported by the intrinsic evidence. The asserted claims themselves, and unasserted claims, discuss allocating "bytes" of memory. For example, asserted claim 5 of the '890 patent recites:

> 5. A method of allocating shared memory in a transceiver comprising:
> transmitting or receiving, by the transceiver, a message during initialization specifying a maximum **number of bytes of memory** that are available to be allocated to a deinterleaver;
> determining, at the transceiver, **an amount of memory** required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data **bytes within a shared memory**;
> allocating, in the transceiver, a first **number of bytes** of the 15 shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for reception at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum **number of bytes** specified in the message;
> allocating, in the transceiver, a second **number of bytes** of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate; and
> deinterleaving the first plurality of RS coded data **bytes within the shared memory** allocated to the deinterleaver and interleaving the second plurality of RS coded data **bytes within the shared memory** allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.

A11 ('890 patent) at claim 5 (emphasis added).[7] Each of the other asserted claims that recite "amount of memory" contain similar disclosures that likewise *only* refer to "bytes." *See* A23 ('381 patent) at claim 5; A35 ('882 patent) at claim 13; A47 ('048 patent) at claim 1. The claim language supports Defendants' proposed construction.

The Family 3 specification speaks of memory in "bytes" too. The Summary of the Invention explains that "a typical DSL transceiver will have at least one latency path with approximately 16 ***kbytes*** of memory for the interleaver." *See* A6 ('890 patent) at 1:43-54. Every example in the specification of sharing memory provides calculations in terms of bytes. *See, e.g.,* A9 ('890 patent) at 6:39-47 ("This latency path will require N*D:128*32:4 ***Kbytes*** of

[7] Defendants reproduce claim 5 as corrected by the certificate of correction.

interleaver memory and the same amount of deinterleaver memory."); *id* at 6:26-33 ("This latency path will require N*D=255*64=16 ***kbytes*** of interleaver memory at the transmitter (or deinterleaver memory at the receiver)."), *id.* at 7:11-25 (similar reference to Kbytes); A10 ('890 patent) at 8:9-19 (calculating total interleaver memory in kbytes), *id.* at 8:29-39 (same).[8] This is consistent with usage in the field. For example, the accused DSL standards refer to memory in terms of bytes. *See* A723-A724 (Jacobsen Decl.) at ¶ 24.

TQ Delta's proposed construction should be rejected because it is a transparent attempt to eliminate claim limitations and thereby broaden claim scope. Neither the specification nor the claims refer to "units" of anything, much less "units of memory." TQ Delta points to extrinsic evidence in the form of a dictionary definition of "bit" to support its construction, but the Family 3 specification does not use "bit" as a measure of an amount of memory, and such a definition is not consistent with the usage in the field. *See* A731-A732 (Jacobsen Decl.) at ¶¶ 44-46.

3. Plaintiff's Reply Position

Defendants transparently ask the Court to limit the claim term "amount of memory" to bytes of memory. To support this unreasonable construction, Defendants contend that because elsewhere the claims recite "a first number of bytes," the Court should construe "an amount of memory" as "number of bytes" as well. This is contrary to the canons of claim construction. When a claim uses different terms, the inference is that the patentee intended "to reflect a differentiation in the meaning of those terms." *Innova/Pure Water, Inc. v. Safari Water Filtration Systems, Inc.*, 381 F.3d 1111, 1119 (Fed. Cir. 2004) ("when an applicant uses different terms in a claim it is permissible to infer that he intended his choice of different terms to reflect a differentiation in the meaning of those terms"); *see also UCB, Inc. v. Accord Healthcare, Inc.*, No. 13-1206-LPS, 2015 WL 2345492, at *6 (D. Del. May 14, 2015) (refusing to give two terms

[8] Kbytes refers to kilobytes.

that appeared in a claim the same meaning because Defendants offered "no persuasive basis to overcome the presumption that the patentee's use of different adjectives in such proximity to one another indicate[d] that the patentee intended the different words to have different meaning."). The claim uses both "amount of memory" and "bytes of memory." Defendants have offered "no persuasive basis" that "amount of memory" and "bytes of memory" should be accorded the same construction. And although the claim will be infringed if the "amount of memory" is specified in bytes, it will also be infringed when the "amount of memory" is specified in other units of memory. The patentee was granted a claim of broader scope. Accordingly, the Court should reject Defendants' attempt to limit the scope of amount of memory.

Defendants argue that because "[t]he Family 3 specification speaks of memory in 'bytes'," the Court should construe "amount of memory" as "bytes of memory." Assuming *arguendo* that the preferred embodiment describes memory in bytes, it is nevertheless improper to read the preferred embodiment into the claims when the claim language is broader. *Liebel–Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004) ("Even when the specification describes only a single embodiment, the claims of the patent will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using 'words or expressions of manifest exclusion or restriction.'") (quoting *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1327 (Fed. Cir. 2002)). Here, the specification does not demonstrate a clear intention to limit the scope of "amount of memory" to bytes.

Finally, Defendants contend that because "the accused DSL standards refer to memory in terms of bytes," amount of memory should construed as bytes of memory. Of course, Defendants cannot point to any law that requires the scope of a claim term to be limited to one particular way of describing an infringing embodiment.

For the foregoing reasons the Court should reject Defendants' construction. TQ Delta also submits that the Court should accord "amount of memory" it's plain and ordinary meaning or in the alternative construe it as "number of units of memory" as TQ Delta proposes.

4. Defendants' Sur-reply Position

Defendants' proposed construction correctly reflects that the specification and claims refer to amounts of memory only in terms of bytes. *Supra* at pp. 51-53. TQ Delta does not dispute that a "number of bytes of memory" can be an amount of memory. TQ Delta makes a conclusory assertion that the claim "will also be infringed when the 'amount of memory' is specified in other units of memory" – without identifying what those units might be, or identifying anything in the intrinsic evidence that would support measuring memory in some other way.

Contrary to TQ Delta's argument, different words ***can*** be found to have the same meaning when the intrinsic evidence shows that was the intent of the patentee. *See Innova/Pure Water, Inc. v. Safari Water Filt. Sys., Inc.*, 381 F.3d 1111, 1119-20 (Fed. Cir. 2004) (ascribing same meaning to "connected" and "associated" where the specification used the words interchangeably in at least one instance, and concluding that "this is simply a case where the patentee used different words to express similar concepts"). And *UCB* is inapposite because the district court in that case made a factual finding that the terms "therapeutic" and "pharmaceutical" are not "used interchangeably in the patent" en route to finding that those terms had different meanings in the claims. *See UCB, Inc. v. Accord Healthcare, Inc.*, C.A. No. 13-1206-LPS, 2015 WL 2345492, at *6 (D. Del. May 14, 2015). Here, the intrinsic evidence

discusses measuring memory only in terms of bytes, which is consistent with the usage in the art. *Supra* at pp. 51-53.[9]

TQ Delta again relies on cases that pre-date *Phillips* to argue that the Court should disregard that the Family 3 specification consistently refers to memory in terms of bytes. However, *Phillips* expressly discouraged TQ Delta's approach because it accorded too little weight to the specification: "Assigning such a limited role to the specification, and in particular requiring that any definition of claim language in the specification be express, is inconsistent with our rulings that the specification is the single best guide to the meaning of a disputed term, and that the specification acts as a dictionary when it expressly defines terms used in the claims or when it defines terms by implication." *Phillips*, 415 F.3d at 1320–21 (internal quotations omitted); *see also Abbott GmbH & Co., KG v. Centocor Ortho Biotech, Inc*., C.A. No. 09-11340-FDS, 2011 WL 948403, at *10 (D. Mass. Mar. 15, 2011) (rejecting approach articulated in pre-*Phillips* cases).

The Court should construe "amount of memory" as "number of bytes of memory."

D. "the shared memory allocated to the [deinterleaver/interleaver] is used at the same time as the shared memory allocated to the [interleaver/deinterleaver]"

Plaintiff's Proposed Construction	Defendants' Proposed Construction
"information is stored in, read from, or written to the shared memory allocated to the deinterleaver at the same time that information is stored in, read from, or written to the shared memory allocated to the interleaver"	*"the deinterleaver reads from or writes to its respective allocation of the shared memory at the same time as the interleaver reads from or writes to its respective allocation of the shared memory"*

[9] While references to measuring memory in terms of bytes in DSL standards are not alone dispositive, such usage confirms that the intrinsic evidence is consistent with the understanding of a person of ordinary skill in the art. The Family 3 specification itself indicates that DSL standards documentation was considered during prosecution (*e.g.*, A2 ('890 patent at 2), citing ITU-T Recommendation G.992.5), and TQ Delta does not dispute that the DSL standards would be consulted by a person of ordinary skill in the art.

1. Plaintiff's Opening Position

The parties competing constructions boil down to whether memory is "used" when "information is stored in, read from, or written to the shared memory," as TQ Delta contends, or only when it is being read from or written to, as Defendants contend. But the primary use of memory is to store information and thus, Defendants construction is unduly narrow.

The IEEE Standard Dictionary of Electrical and Electronics Terms considers storage as a synonym of memory and defines it as ". . . any device in which information can be *stored*, sometimes called a memory device" or "the physical means of *storing* information A89-90 (IEEE Standard Dictionary of Electrical and Electronics Terms, 4th ed. (1988) at p 582 ("memory. See: storage") and p. 956 (defining storage as "[a]ny device in which information can be *stored*, sometimes called a memory device") (emphasis added)); see also A100-101 (Standard Dictionary of Computers and Information Processing, Martin H. Weik, 3rd printing (1970) at p. 186 (stating that memory is same as storage) and p. 271 (defining storage as "[a] device . . . which receives data, *holds* and, at a later time, returns data.") (emphasis added); See also A687 (Cooklev Decl.) at ¶ 35. Thus, it is incontrovertible that memory is used to *store* information. TQ Delta's construction accounts for this irreducible minimum "use" of memory. Defendants' construction on the other hand leaves out the primary "use" of memory – storage. The Court should adopt TQ Delta's construction that correctly accounts for what "using" memory means.

2. Defendants' Answering Position

Contrary to TQ Delta's characterization of the dispute, the issue is not whether any generic memory can, in the abstract, be "used" to store information, but how allocated shared memory is "used" in the context of the claims.

Defendants' proposed construction correctly reflects that the shared memory is read to

and written from *at the same time* by the interleaver and the deinterleaver. Defendants' proposed construction is consistent with the specification, which discloses that "the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory and the shared memory can be allocated to the interleaver and/or deinterleaver of each latency path." A7 ('890 patent) at 4:1-13; *see also id*. at 4:57-65. The asserted claims clearly indicate that the shared memory allocated to the deinterleaver "is used at the same time" as the shared memory allocated to the interleaver. *See, e.g*., A11 ('890 patent) at claim 5; A23 ('381 patent) at claim 5; A35 ('882 patent) at claim 13; A47 ('048 patent) at claim 1.

The prosecution history supports Defendants' construction as well. During prosecution, in an interview with the examiner, the applicant explained that the invention had "features of ***simultaneous transfer*** and types of interleaving and allocation of memory based on direction of transmission and bandwidth." A167 (D.I. 312, Ex. H) (emphasis added). The "at the same time" language was later added via an Examiner's amendment. *See* A178-79 (D.I. 312, Ex. H). Simultaneous transfer requires the active steps of reading to and writing from memory; passive storage, as contemplated by TQ Delta's proposed construction, would not achieve simultaneous transfer. *See* A734 (Jacobsen Decl.) ¶ 51.

TQ Delta's proposed construction is another attempt to broaden the claims by including mere storage of data in memory as a use of memory, despite the prosecution history admission of "simultaneous transfer." A167 (D.I. 312, Ex. H). Under TQ Delta's construction, a device could infringe as long as the portion of memory allocated to the interleaver and the portion of memory allocated to the deinterleaver were both storing some information—even if that information were stale (*e.g.*, from a previous connection). Neither portion of the memory would actually have to be used, or accessed by a deinterleaver or interleaver function at all, because some information

would be "stored" in the memory regardless of whether a particular latency path is active. This is contrary to the plain meaning of "at the same time" and the concepts of shared memory according to the specification. TQ Delta's attempt to sow confusion by introducing an artificial distinction between allocated memory and used memory has no bearing on the parties' claim constructions, and as discussed above, is unsupported by the intrinsic evidence.

TQ Delta's construction relies exclusively on extrinsic evidence. The Court should adopt Defendants' construction, and reject TQ Delta's attempt to rewrite the claims with extrinsic evidence.

3. Plaintiff's Reply Position

As an initial matter, technical dictionaries cited by TQ Delta amply support TQ Delta's contention that shared memory is "used" when "information is stored in, read from, or written to the shared memory." This is the plain and ordinary meaning of what it means to "use" memory. Defendants do not dispute this. Instead, Defendants argue that the prosecution history somehow limits the scope of "use" to only "reads from or writes to," and importantly excludes "store." There is no merit to this argument.

Specifically, Defendants argue that because during an examiner interview "the applicant explained that the invention had 'features of simultaneous transfer and types of interleaving and allocation of memory based on direction of transmission and bandwidth,'" the scope of "used" is restricted to the simultaneously reading and writing of memory. For the Court's convenience, the entirety of the interview is summary is reproduced below.

Continuation of Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: The examiner and applicant discussed an overview of the invention and explained features of simultaneous transfer and types of interleaving and allocation of memory based on direction of transmission and bandwidth. The examiner felt the proposed amendment was a step in the right direction but that more details would be recommended to overcome the cited prior art. The examiner suggested the features of need more detailing such as type of memory, type of interleaving to distinguish from the prior art or memory art. .

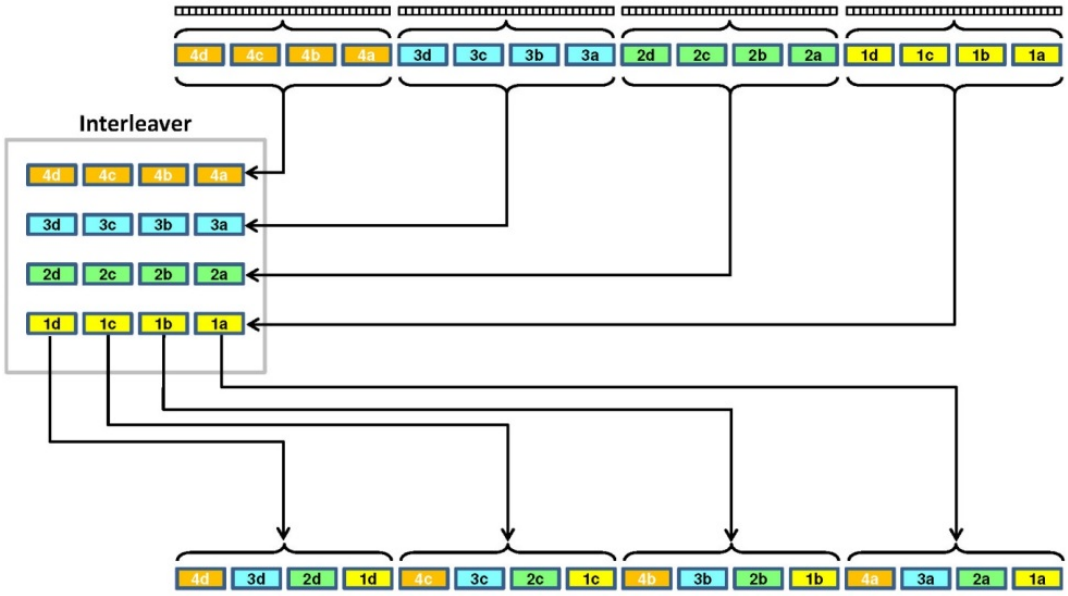
As explained by Dr. Cooklev, Defendants and their expert incorrectly interpret the words "simultaneous transfer" in the interview summary as referring to transfer to and from the shared memory. A754-A755 (Cooklev Reply Decl.) at ¶ 24. There is no basis for concluding that the referenced "transfer" is to and from memory. *Id*. The examiner's summary does not state that the transfer is to/from memory and the Family 3 patent specification does not use the term transfer in describing use of the memory. *Id*. To arrive at the incorrect, self-serving conclusion that the "simultaneous transfer" bears on the use of shared memory, Defendants disregard the context of the interview summary.

When viewed in context of the other patent office communications, the examiner's reference to "simultaneous transfer" is referring to the fact that transmission and reception of data are occurring simultaneously and, therefore, the shared memory is being used concurrently by the interleaver and deinterleaver. *Id*. Specifically, this interpretation of the examiner's statement is supported by the fact that the Office Action that the examiner issued on the day after the examiner interview identifies as a primary topic "how the same memory can be used for simultaneously receiving of data and transmitting data" and states "it is noted that the features upon which applicant relies (i.e., the same memory being used for simultaneously receiving of data and transmitting data) are not recited in the claims." *Id*. (citing A148 (12/9/2009 Office Action at p. 2)). Just as in the examiner's interview summary, there is no discussion in the Office Action of simultaneous transfer to/from memory.

Further, to the extent Defendants contend that the simultaneous transmission and reception of data necessarily requires that "the interleaver would need to be able to read from or write to the shared memory at the same time the deinterleaver was reading from or writing to the shared memory, Defendants are mistaken. A755 (Cooklev Reply Decl.) at ¶ 25. All that is

required is that the shared memory can be used simultaneously by the interleaver and deinterleaver. *Id*. Consequently, memory is being "used" by an interleaver or deinterleaver function when the memory is passively storing, in addition to actively reading or writing, data relating to the function. *Id*.

The use of memory for the passive act of storing (i.e., temporarily holding) data while it is being interleaved is an integral part of the function of interleaving. A755 (*Id.*) at ¶ 26 (citing Cooklev Decl. at ¶¶ 16-32). Dr. Jacobsen agreed with this explanation. *Id*. (citing A720 (Jacobsen Decl.) at ¶ 16). An illustration of a simple interleaver that was previously set forth in Dr. Cooklev's opening declaration is reproduced below.



As Dr. Cooklev explains, using the memory to store data is an integral part of interleaving:

> 27. As I explained in my prior declaration, "the first groups of bits from the four different codewords (yellow #1a, green #2a, blue #3a, and orange #4a) is transmitted first; then a second group of bits from each codeword (yellow #1b, green #2b, blue #3b, and orange #4b) are transmitted and so on." A_ (Cooklev Decl.) at ¶ 25. In DSL the block of codewords is transmitted serially transmitted as a serial stream of DMT symbols. Thus, a non-infinitesimally small amount of time elapses before the transmission of the four groups of bits is complete. During this time, the groups of bits are stored in the interleaver memory. This storage is

> necessary so that the order of the groups of bits can be rearranged (i.e., interleaved). Thus, a POSITA would understand that, with regards to the interleaver, use of memory in the context of the claims would include reading, writing and storing of information.

A756 (Cooklev Reply Decl.) at ¶ 27. Using the memory for storing data is also an integral part of deinterleaving:

> 28. With respect to the deinterleaver at the receiver, as I previously stated "the first group of yellow bits (yellow #1a) must be stored while waiting for the second group (yellow #1b), third (yellow #1c), and fourth group (yellow #1d) of yellow bits to be received. Only after receipt of all of the bits of a codeword can the codeword be decoded." A683-A684 (Cooklev Decl.) at ¶ 27. While the deinterleaver is waiting for all groups of bits for a given codeword to be received, the already received group of bits is stored in deinterleaver memory. This is necessary so that the groups of bits may be arranged back into their original order. Thus, a POSITA would understand that, with regards to the deinterleaver, use of memory in the context of the claims would include reading, writing and storing of information.

A756-A757 (Cooklev Reply Decl.) at ¶ 28. Thus, when interleaving of data for transmission is being performed at the same time as deinterleaving of received data, the portion of the memory used by the interleaver is being used at the same time as the portion of the memory used by the deinterleaver.

Defendants' expert constructs a hypothetical example to attempt to illustrate that under TQ Delta's construction a memory location that "stores stale information would" nevertheless meet TQ Delta construction. But this hypothetical mischaracterizes what it means to use memory by storing information. A757 (Cooklev Reply Decl.) at ¶ 29. As Dr. Cooklev explains:

> Memory is used for storage by an interleaver or deinterleaver when the memory stores information waiting to be transmitted, or stores received information that has not been processed. Once the information is transmitted or processed, the information is no longer relevant and the interleaver/deinterleaver can use the same memory to store the next block of information to be interleaved or deinterleaved. A POSITA would recognize that once the information in the memory is transmitted or processed, it is no longer being "used" by the interleaver or deinterleaver. Stale information is not used and, consequently, the memory that is storing the stale information is no longer being used by the interleaver or deinterleaver.

Id. For these reasons, this Defendants' hypothetical is technically inaccurate and irrelevant.

The Court should reject Defendants attempt to restrict the term "memory . . . is used" only to use of the memory by reading from or writing to the memory. Instead, the Court should adopt TQ Delta's proposed construction which follows the plain and ordinary meaning of "memory . . . is used," which as Defendants admit includes storing in the memory.

4. Defendants' Sur-reply Position

TQ Delta initially disputed that the portions of memory had to be "used" at the same time by suggesting that mere storage of information in memory constituted "use" of the memory. In its Reply Brief, TQ Delta backtracks from that untenable position and suggests that the "storage" within the scope of its proposed construction is limited to use of the memory while the interleaver or deinterleaver is processing the data. According to TQ Delta, "a non-infinitesimally small amount of time elapses before the transmission of the four groups of bits is complete. During this time, the groups of bits are stored in the interleaver memory." A756 (Cooklev Reply Decl.), ¶ 27. Thus, TQ Delta now concedes that "use" refers to the small amount of time that information is stored so that groups of bits can be interleaved or deinterleaved. *See* A756-A757 (Cooklev Reply Decl.), ¶¶ 27-28. This brings the parties' understanding closer.

TQ Delta's proposed construction, however, does not reflect the explanation in its Reply Brief. A person of ordinary skill in the art would not understand "information… stored in" to include only information stored for a "non-infinitesimally small amount of time" while it is actually being interleaved or deinterleaved. A761 (Jacobsen Reply Decl.), ¶¶ 6-7. Accordingly, Defendants propose the following compromise position – "the deinterleaver reads from, writes to or stores information for deinterleaving in its respective allocation of the shared memory at the same time as the interleaver reads from, writes to, or stores information for interleaving in its respective allocation of the shared memory."

In its Reply Brief, TQ Delta misinterprets the file history to try to save its overbroad proposed construction. TQ Delta argues that the discussion of "features of simultaneous transfer…" between the Examiner and the applicant during prosecution did not refer to the use of memory, but instead transferring data, because the Office Action issued in connection with the interview indicates that simultaneous use of a shared memory was not recited in the claims then at issue. *Supra* at pp. 59-60. TQ Delta ignores that in response to this Office Action, the Applicant then amended the claims to refer to simultaneous memory use. *Compare* A658-662 (Amdmt. and Resp., 8/21/2009), at 3 *with* A648 (Amdmt. and Resp., 12/17/2009), at 2 (adding "wherein the shared memory is used to simultaneously interleave the first plurality of RS coded data bytes and deinterleave the second plurality of RS coded data bytes"). Based on the similarities between claim 46 and the asserted claims, and the fact that neither says anything about "simultaneously receiving of data and transmitting data," the necessary implication is that the discussed "simultaneous transfer" did indeed refer to the use of the shared memory to "simultaneously interleave the first plurality of RS coded data bytes and deinterleave the second plurality of RS coded data bytes." As a person having ordinary skill in the art at the time of the alleged invention would have understood, being able to "simultaneously interleave . . . and deinterleave" would require the interleaver to be able to read from or write to the shared memory at the same time the deinterleaver is reading from or writing to the shared memory. *See* A761-A763 (Jacobsen Reply Decl.), ¶¶ 8-11.

The Court should adopt Defendants' proposed construction for this term.

E. "latency path"

Plaintiff's Proposed Construction	Defendants' Proposed Construction
"a transmit or receive path, each path associated with a latency"	*"distinct transmit or receive path"*

1. Plaintiff's Opening Position

The parties agree that the term "path" corresponds to a "transmit or receive path." Defendants however fail to account for the term "latency" in their construction. Thus, under the guise of providing a construction for "latency path," Defendants ask the Court to rewrite the claim by omitting the term "latency." This is improper. The Court should decline Defendants' invitation to rewrite the claims.

Plaintiff's construction on the other hand accounts for the term latency. At least for this reason, Plaintiff's construction should be adopted over Defendants' construction. *See Merck & Co. v. Teva Pharm. USA, Inc.*, 395 F.3d 1364, 1372 (Fed. Cir. 2005) (noting that "[a] claim construction that gives meaning to all the terms of the claim is preferred over one that does not do so.").

2. Defendants' Answering Position

The parties agree that "latency path" means "transmit or receive path" but dispute whether the latency path is a *distinct* and separate path from another latency path.

Defendants' proposal that the transmit or receive path be "distinct" is supported by the intrinsic evidence. The claims that use the term clearly refer to distinct paths, *e.g.*, a "first" and a "second" latency path. *See* A61 ('473 patent) at claim 19 ("a multicarrier communications transceiver that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path"), *id.* at claim 28 ("a multicarrier communications transceiver that is configured to generate a message during an initialization of the transceiver, perform an interleaving function associated with a first latency path, and perform a deinterleaving function associated with a second latency path"), A73 ('126 patent) at claim 1 ("a multicarrier communications transceiver that is configured to

perform a first interleaving function associated with a first latency path and perform a second interleaving function associated with a second latency path"), A74 ('126 patent) at claim 10 ("a multicarrier communications transceiver that is configured to generate a message during an initialization of the transceiver, perform a first deinterleaving function associated with a first latency path, and perform a second deinterleaving function associated with a second latency path"). The specification likewise describes distinct paths. *See, e.g.*, A7 ('890 patent) at 4:41-51 ("Each of the latency paths in the transmitter portion 200 includes a framer, coder, and interleaver designated as 212, 214, 216 and 222, 224 and 226, respectively. Each of the latency paths in the receiver portion includes a deframer, decoder, and deinterleaver designated as 312, 314, 316 and 322, 324, and 326, respectively."). Both the claims and the specification support Defendants' proposed construction. *See* A735-A736 (Jacobsen Decl.) at ¶ 55.

TQ Delta's opening brief does not acknowledge this aspect of the parties' dispute, much less provide any rationale for construing latency path as "a" transmit or receive path. Accordingly, the Court should adopt Defendants' proposed construction.

TQ Delta argues that Defendants' construction does not "account for the term 'latency.'" *Supra* at p. 65. But a person of ordinary skill in the art would understand that transmit/receive paths have latencies (*i.e.*, delays), so Defendants' construction inherently accounts for the term latency. *See* A735 (Jacobsen Decl.) at ¶ 54.[10] TQ Delta's proposal that each path is "associated with a latency" merely repeats a term to be construed ("latency") without clarifying what it means. The '890 patent explicitly defines latency as delay. *See* A6 ('890 patent) at 1:24-26

[10] Defendants maintain their construction is sufficient. In the interests of narrowing the dispute, however, if necessary, Defendants would be willing to clarify their original proposed construction of "latency path" to add at the end of Defendants' proposed construction ". . . wherein each path is associated with a delay."

("DSL systems carry applications that have different transmission requirements with regard to, for example… latency (delay)").

3. Plaintiff's Reply Position

The claim term recites "latency path"; Defendants' construction does not account for the word latency in any way. Defendants attempt to excuse this deficiency by arguing that "a person of ordinary skill in the art would understand that transmit/receive paths have latencies (i.e., delays), so Defendants' construction *inherently* accounts for the term latency." *See supra* at p._ (emphasis added). Irrespective of whether the technical point is accurate, Defendants' understanding that something is inherent to one of skill in the art will not help the fact finders. The scope of the claims by which the Court and jury will evaluate infringement and validity should be memorialized in the Court's claim construction and should be explicit. Additionally, the Court should adopt TQ Delta's construction to forestall any attempt by Defendants to later argue that this claim element is taught by a prior art reference that lacks disclosure of a path associated with a latency.

Separately, Defendants complain about TQ Delta's use of the indefinite article, "a" in "a transmit or receive path." Instead, of the indefinite article "a," Defendants propose using the term "distinct." But, there is no good reason for adding the word "distinct" to the claims, and the inclusion of "distinct" may cause confusion. The claims that include the term "latency path" recite "a first latency path" and "a second latency path." The words "first" and "second" already sufficiently denote that there are two latency paths, not only a single latency path. The word "distinct" does not clarify this issue.

On the other hand, the word "distinct" may cause unnecessary confusion. While each latency path described in the Family 3 specification will have some distinct aspects to it (for example, each path may have a distinct latency because the coding and interleaving parameters

for each path are separately configurable), other aspects of the latency path are not distinct at all. For example, in a first example embodiment, the latency path used for transmission and the latency path used for reception are transmitted and received by the same transceiver using shared memory. A8 ('890 patent) at, *e.g.*, 6:11-15 ("Three examples of sharing interleaver/deinterleaver memory and coding processing in *a transceiver* are described below. The latency paths in these examples can be in the transmitter portion of *the transceiver* or the receiver portion of *the transceiver*."); and 5:33-39 ("For example, an exemplary transceiver could comprise a shared interleaver/deinterleaver memory and could be designed to allocate a first portion of the shared memory 120 to an interleaver, such as interleaver 216 in the transmitter portion of *the transceiver* and allocate a second portion of the shared memory 120 to a deinterleaver, such as 316, in the receiver portion of *the transceiver*.") (emphasis added). In a second example embodiment, two latency paths, both of which are used for transmission, are transmitted by the same transceiver using shared memory. A8 ('890 patent) at, *e.g.*, 5:40-46 ("Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory, such as shared memory 120, and be designed to allocate a first portion of shared memory 120 to a first interleaver, e.g., 216, in the transmitter portion of *the transceiver* and allocate a second portion of the shared memory to a second interleaver, e.g., 226, in the transmitter portion of *the transceiver*.") (emphasis added). In this sense, the latency paths are not distinct at all. A claim construction that requires the paths to be "distinct" could confuse the jury into finding non-infringement for an improper reason.

For the foregoing reasons, the Court should refuse to include the term "distinct" in its construction. The Court should construe "latency path" as "transmit or receive path, each path associated with a latency," as TQ Delta proposes.

4. Defendants' Sur-reply Position

TQ Delta fails to respond to Defendants' offer to narrow the dispute (*Supra* at p. 66) by adding clarifying language at the end of their proposal, as follows: "distinct transmit or receive path, *wherein each path is associated with a delay*." That proposal should moot any concerns about explicitly accounting for the term "latency" (which was inherently reflected in Defendants' original construction).

Defendants' proposed construction does not introduce ambiguity into the meaning of the claim terms as TQ Delta argues. The concept of distinct paths is clear to one of ordinary skill in the art. TQ Delta essentially argues that confusion could arise because multiple distinct paths may be included in a single transceiver. TQ Delta's argument refers to the transceiver, not the paths themselves, which TQ Delta concedes are distinct from one another. Nothing in Defendants' proposed construction suggests, for example, that multiple paths cannot go to and from the same transceiver.[11] Defendants' proposal simply reflects that the claims clearly refer to "first" and "second" latency paths, and the specification likewise describes distinct paths. *Supra* at pp. 65-66.

F. "wherein at least a portion of the memory may be allocated to the [first] interleaving function or the [second interleaving / deinterleaving] function at any one particular time depending on the message"

Plaintiff's Proposed Construction	Defendants' Proposed Construction
"at least some particular memory cells within the memory can be allocated for use by either the [first] interleaving function or [second interleaving / deinterleaving] function at any one particular time depending on the	*"wherein at least a number of bytes within the memory may be allocated to the [first] interleaving function or the [second interleaving / deinterleaving] function at any one particular time depending on the amounts*

[11] TQ Delta also seems to agree that the references to "a" and "the" transceiver in the specification refer to a single transceiver (*supra* at pp. 67-68), which undermines its argument that the specification's references to "a" and "the" shared memory do not refer to a single shared memory. *See* Section VI.B.1, *supra*.

message"	*of memory specified in the message"*

1. Plaintiff's Opening Position

This is another attempt by Defendants to constrain a term to a quantum of memory specified in bytes. Defendants urge the Court to construe "a portion of memory" as "a number of bytes" and further ask the Court to require that the claimed "message" specify "the amounts of memory." Nothing in the specification supports Defendants' contention that an "amount of memory" be specified in the message. In fact, the specification contemplates that the message can include different types of information that can be used to perform the allocation. *See* A10 ('890 Patent) at 9:14-19 ("Moreover, the messages received from the other transceiver could specify what the memory allocation is to be based on, for example, the number of latency paths, memory allocation in the remote transceiver and required applications."). Therefore, Defendants' attempt to limit the scope of message is improper. *See Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004) (noting that "[e]ven when the specification describes only a single embodiment, the claims of the patent will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using 'words or expressions of manifest exclusion or restriction.'") (citations omitted). At least for this reason, the Court should reject Defendants' construction.

The Court should also reject Defendants' construction that equates the claimed "portion of memory" to "a number of bytes," because it is wrong. Specifically, the claim limitation calls for the allocation of "a portion of the memory" "to the [first] interleaving function or the [second interleaving / deinterleaving] function at any one particular time." As previously explained, the interleaver and deinterleaver perform interleaving and deinterleaving in different physical portions (i.e., memory cells) of the memory. Specifically, because the interleaver is interleaving

codewords ready for transmission and the deinterleaver is deinterleaving a received interleaved codewords, it is technically impossible for the interleaver and the deinterleaver to use the same physical locations (memory cells) of memory at the same time. This claim limitation clarifies that requirement by construing portion of memory as the physical memory cells allocated to a function (interleaver to deinterleaver).

Defendants' construction on the other hand leads to nonsensical results. Specifically, under Defendants' construction if "a number of bytes," 10 bytes for example, was allocated to the interleaver, the deinterleaver cannot be allocated the same "number of bytes," i.e., 10 bytes for example. Nothing in the specification calls for this result, i.e., that the interleaver cannot be allocated the same number of bytes as the deinterleaver.

2. Defendants' Answering Position

The parties' dispute regarding whether memory is measured in terms of bytes is addressed in Defendants' discussion of the term "amount of memory" above. *See* Section VI.C. Defendants' proposal additionally reflects that the allocation between the first and second functions (*e.g.*, interleaving and deinterleaving) is based on the amounts of memory specified in the message.

TQ Delta argues incorrectly that Defendants' construction would require "the interleaver and the deinterleaver to use the same physical locations (memory cells) of memory at the same time." *Supra* at pp. 70-71. Again, TQ Delta attempts to import a "memory cell" concept that has no basis in the intrinsic record. Nowhere do the Family 3 patents talk about "memory cells." And Defendants' proposed construction has nothing to do with requiring an interleaver to use the same physical locations at the same time. Defendants' construction merely requires that the interleaver and deinterleaver share memory— *i.e.*, the interleaver can read from or write to its memory allocation at the same time the deinterleaver can read from or write to its memory

allocation. *See* A739 (Jacobsen Decl.) at ¶ 60. Defendants' construction identifies how memory is measured but does not place any restrictions on the number of bytes of memory that may be allocated, so it would not prohibit allocating the same number of bytes to each of the interleaver and the deinterleaver.

The parties also disagree regarding the content of the claimed message. Defendants' proposed construction is supported by the intrinsic record, including the claim language itself, which requires that the amount of memory be allocated as specified in the message. Moreover, the corresponding limitations in A61 ('473 patent) at claim 28 and A74 ('126 patent) at claim 10 recite: "wherein the generated message indicates how the memory has been allocated between the [first deinterleaving / interleaving] function and the [second] deinterleaving function." If some other parameter (such as latency) were the information exchanged, the message would not be able to indicate how the memory has been allocated. *See* A737-A738 (Jacobsen Decl.) at ¶ 59. Accordingly, allocation depends on the amount of memory specified in the message. *Id*. No other embodiments are recited in the asserted claims that contain this limitation. *See* A61 ('473 patent) at claim 19; A73 ('126 patent) at claim 1. Moreover, the specification indicates that the amount of memory is the minimum information that the message contains. *See, e.g*., A9 ('890 patent) at 8:59-9:3 ("a maximum amount of shared memory that can be allocated to a specific interleaver or deinterleaver… is determined," and then "the determined maximum amount… is transmitted to another transceiver." "Messages containing additional information can also be transmitted…").

TQ Delta's proposed construction should be rejected because it is another transparent attempt to broaden the claims through claim construction to try to capture clearly non-infringing technology. *See, e.g., Wilson Sporting Goods Co. v. Hillerich & Bradsby Co.*, 442 F.3d 1322,

1326-27 (Fed. Cir. 2006) (recognizing that "knowledge of [an accused] product or process provides meaningful context for the first step of the infringement analysis, claim construction."). TQ Delta contends that the "O-PMS message" in the DSL standard infringes this claim. The O-PMS message does not specify any number of bytes of memory. Instead, it contains information on maximum delay for a latency path in octets. *See* A515-30 (excerpt of '473 inf. Contentions); *see also* A541-552 (Excerpt of ITU-T G.993.2 (2/2006) at § 12.3.5.2.1.3). This is why TQ Delta is trying, through claim construction, to empty the claimed message of any content. But the claimed content of the message was the exact point of novelty identified by the examiner that made the claim allowable. The intrinsic evidence defeats TQ Delta's gambit. Accordingly, the Court should adopt Defendants' proposed construction.

3. Plaintiff's Reply Position

The parties have two disputes: (1) the meaning to ascribe to a "portion of the memory" and (2) the meaning to ascribe to "memory may be allocated . . . depending on the message."

First, with respect to "portion of memory," TQ Delta's construction – "particular memory cells" – attempts to clarify that separate respective physical portions of the memory or separate respective memory locations within the memory are allocated to either the interleaver or deinterleaver. Based off Defendants' response and their expert's declaration, it appears that Defendants agree that "portion of memory" refers to physical locations in the memory and not simply a quantum of memory. *See* A739 (Jacobsen Decl.) at ¶ 60; A748-A749 (Cooklev Reply Decl.) at ¶ 8. Dr. Jacobsen also notes that "the interleaver can read from/write to its memory allocation at the same time the deinterleaver can read from/write to its memory allocation" (A739 (Jacobsen Decl.) at ¶ 60) indicating that the interleaver and deinterleaver are allocated their respective "portion of memory." However, Defendants' construction – "at least a number of bytes within the memory" does not clarify that "portion of memory" corresponds to distinct

physical locations in the memory. In fact, Defendants' construction could be interpreted to simply mean a quantum of memory. TQ Delta's construction on the other hand avoids the ambiguity of Defendants' construction.

Defendants and Dr. Jacobsen's argument that "it is unclear whether TQ Delta considers 'memory' to be physical memory or addresses corresponding to, but divorced from, physical memory locations" (A737 (Jacobsen Decl.) at ¶ 57) is irrelevant on its face because the argument concedes, as it must, that both physical memory (i.e., memory cells) and memory addresses correspond to *physical* memory. For example, when memory addresses are allocated to the interleaving function, this is the same as the allocation to the interleaving function of the physical memory cells that correspond to the memory addresses.

Second, Defendants ask the Court to construe "memory may be allocated . . . depending on the message" as "memory may be allocated . . . depending on the amounts of memory specified in the message." Nothing in the claims or the specification requires that the amounts of memory be specified in the message. For example, claim 1 of the '126 patent recites:

> 1. An apparatus comprising:
> a multicarrier communications transceiver that is configured to perform a first interleaving function associated with a first latency path and perform a second interleaving function associated with a second latency path, the multicarrier communications transceiver being associated with a memory,
> wherein the memory is allocated between the first interleaving function and the second interleaving function in accordance with a message received during an initialization of the transceiver and wherein at least a portion of the memory may be allocated to the first interleaving function or the second interleaving function at anyone particular time depending on the message.

Thus, on its face the claim merely requires, in relevant part, the allocation of a portion of the memory to one of the functions "depending on the message." Nothing in the claim requires the message to specify "amounts of memory."

Nor does the specification disclaim a broader scope of the word "message." The Defendants' expert points to examples in the Family 3 Patents where a message may specify an amount of memory (A737-A738 (Jacobsen Decl.) at ¶ 59), but some of the examples are referring to a total amount of memory that a transceiver (or modem) has, not an amount to be allocated to a particular function. And none of these examples state that a message must specify "amounts of memory"; rather, the examples are referring to what a particular transceiver "must know." A transceiver may know sufficient information to allocate portions of memory without the message specifying "amounts of memory." For example, the Family 3 patents explain with respect to Figure 4 that the message may contain, more generally, "latency path information (FCI block information)" and "additional information" that can be used in "the determination of memory allocation." A9 ('890 patent) at 9:8-14. "Moreover, the messages received from the other transceiver could specify what the memory allocation is to be based on, for example, the number of latency paths, memory allocation in the remote transceiver and required applications." *Id.* at 9:14-17.

In view of the foregoing, a construction that requires the message to specify "amounts of memory" is not proper.

To distract the Court from their attempt to read limitations into the claims, Defendants accuse TQ Delta of attempting to broaden the claims "to try to capture clearly non-infringing technology." This accusation is meritless.

As previously explained, the claims and the specification do not require that the message "specify" an "amount of memory." Therefore, TQ Delta's construction only seeks the scope conferred by the plain meaning of the words actually found in the claims – nothing less and

nothing more. TQ Delta is not attempting to "empty the contents of message," as Defendants contend. Instead, Defendants are seeking to force specific content into the message.

For the foregoing reasons, the Court should reject Defendants' construction.

4. Defendants' Sur-reply Position

The parties' dispute regarding whether memory is measured in terms of bytes is addressed in Defendants' discussion of the term "amount of memory" above. *See* Section VI.C. The parties' dispute regarding TQ Delta's attempt to define shared memory in terms of "particular memory cells" is addressed in Defendants' discussion of the term "shared memory" above. *See* Section VI.D, ***supra.*** The remainder of the parties' dispute focuses on the *content* of the claimed message.

Regarding the content of the message, the intrinsic record shows that the message must specify at least an amount of memory (although it may also specify other parameters as well). *Supra* at pp. 72-73. The prosecution history shows that the content of the message was the only basis for allowance. Thus, if the claims were construed such that a message need not specify an amount of memory, the claims would read on the prior art. TQ Delta's argument attempts to distract from the fact that the claimed content of the message was the feature that made the claim allowable. *See* A150-152, 154-155 (Office Action, 12/9/2009); A173-181 (Not. of Allow., 9/7/2010) ("The closest prior art, Fadavi-Ardekani et al (U.S. Pat. 6,707,822) discloses sharing a memory between the interleavers and deinterleavers of multiple ADSL sessions, fails to suggest limiting the memory allocated to the interleaver to a maximum number of bytes available that was specified in a transmitted or received message."). Contrary to TQ Delta's argument, the specification does not provide any way for a transceiver to allocate portions of memory if the message does not specify an amount of memory to allocate. *See* A763-A764 (Jacobsen Reply Decl.), ¶¶ 12-13. The specification repeatedly states that the message specifies an amount of

memory. *See, e.g.*, A7 ('890 patent), col. 4:24-28 ("a first transceiver and a second transceiver transmit to one another messages during, for example, initialization which contain information on the total and/or shared memory capabilities of each transceiver and optionally information about the one or more latency paths."); A9 ('890 patent), col. 8:9-21 (stating that message sent by first transceiver to second transceiver during initialization contains "Max Interleaver Memory" for latency paths #1, #2, and #3, and "Maximum total/shared memory for all latency paths," and that first transceiver "select[s] latency path settings" based on this information); *id*. at col. 8:47-51 (same); *id*. at col. 8:62-67 ("a maximum amount of shared memory that can be allocated to a specific interleaver or deinterleaver of a plurality of interleavers or deinterleavers in a transceiver is determined. Next, in step S320, the determined maximum amount for one or more of the deinterleavers and/or interleavers is transmitted to another transceiver.").

To support its construction, TQ Delta asserts that some examples in the specification refer to what a particular transceiver "must know" instead of specifying an amount of memory in a message. TQ Delta is apparently alluding to statements within Example #3 stating that "the first modem must know the maximum amount of interleaver memory for each transmitter latency path" and "the first modem must know the total shared memory for all transmitter latency paths." A9 ('890 patent), col. 8:1-5. TQ Delta ignores that the specification then immediately explains that the purpose of this knowledge is for the first modem to meet application requirements and "meet the transmitter portion latency path capabilities of the second modem." *Id*. at col. 8:5-8. The specification then immediately illustrates how "a first transceiver could send a message to a second transceiver during initialization or during SHOWTIME containing the following information," which includes "Max Interleaver Memory for [each] latency path," measured in bytes, and "Maximum total/shared memory for all latency paths," also measured in bytes. *Id*. at

col. 8:9-39. TQ Delta also points to the portion of the specification describing Figure 4. *Id*. at col. 9:4-17. Figure 4 describes a procedure for "resource sharing" that may be based on parameters such as the number of latency paths. *Id*. But the only "resource" at issue in the claims here is memory. And when the "resource" of Figure 4 is memory, the specification states that the message specifies "memory allocation." *Id*. at col. 9:12-18.

Defendants' proposed construction is thus consistent with the intrinsic record, including the only point of novelty that made the claim allowable during prosecution. The Court should adopt Defendant's proposed construction.

G. "portion of the memory"

Plaintiff's Proposed Construction	Defendants' Proposed Construction
This term should not be construed out of context. See above for proposed construction in context.	*"number of bytes within the memory"*

1. Plaintiff's Opening Position

TQ Delta submits that "proper construction [of this phrase] requires consideration of the context of the rest of the term." *See Ultimax Cement Mfg. Corp. v. CTS Cement Mfg. Corp.*, 587 F.3d 1339, 1347 (Fed. Cir. 2009); *see also, ACTV, Inc. v. Walt Disney Co.*, 346 F.3d 1082, 1088 (Fed. Cir. 2003) (noting that "[w]hile certain terms may be at the center of the claim construction debate, the context of the surrounding words of the claim also must be considered in determining the ordinary and customary meaning of those terms.") Accordingly, this term should be construed within the context of the entire element as set forth in *supra* at VI. F.

2. Defendants' Answering Position

As with other terms addressed above, the parties' dispute centers around how to quantify the claimed memory. Defendants' proposal that "portion of memory" be construed as "number

of bytes within the memory" is consistent with the intrinsic evidence, and is the only way that the specification quantifies memory. The specification states that "the allocation module 150 allocates a portion of the shared memory 120 to one or more of the interleaver and/or deinterleavers, or groupings thereof." A8 ('890 patent) at 5:58-6:11. As discussed above with respect to "amount of memory," the Family 3 specification refers to memory only in terms of bytes or kilobytes. *See, e.g.,* A6 ('890 patent) at 1:43-54, A8 ('890 patent) at 6:26-33, 6:39-47, A9 ('890 patent) at 7:11-25; *see also* A11 ('890 patent) at claim 5 ("bytes within a memory"). Claim 5 of the '890 patent, which is a method claim similar to the asserted claims, indicates that bytes are "within" the memory. *See* A11 ('890 patent) at claim 5 ("deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the inter leaver").

TQ Delta contends that this term should not be construed "out of context." But nothing in the larger "wherein" clause requires "portion of the memory" to mean "some particular cells within the memory" as TQ Delta's construction would require. Again, the Family 3 patents do not discuss the concept of "cells within the memory" at all. This is an entirely new concept being injected by TQ Delta to try to change the meaning of the claims.

3. Plaintiff's Reply Position

TQ Delta reiterates that "proper construction [of this phrase] requires consideration of the context of the rest of the term." *See Ultimax Cement Mfg. Corp. v. CTS Cement Mfg. Corp.*, 587 F.3d 1339, 1347 (Fed. Cir. 2009); *see also, ACTV, Inc. v. Walt Disney Co.*, 346 F.3d 1082, 1088 (Fed. Cir. 2003) (noting that "[w]hile certain terms may be at the center of the claim construction debate, the context of the surrounding words of the claim also must be considered in determining

the ordinary and customary meaning of those terms.") Accordingly, this term should be construed within the context of the entire element as set forth in *supra* at VI. F.

4. Defendants' Sur-reply Position

There is no reason the term "portion of the memory" cannot be construed as an individual phrase. Nothing in the larger "wherein" clause above requires "portion of the memory" to mean "some particular cells within the memory" as TQ Delta's construction would require.

The cases TQ Delta relies upon do not support avoiding construction of this term, or importing limitations based only on extrinsic evidence. In *Ultimax Cement*, the Federal Circuit determined that that the term "anhydride" in the phrase "soluble $CaSO_4$ anhydride" was "intended as a modifier" of the term $CaSO_4$. *Ultimax Cement Mfg. Corp. v. CTS Cement Mfg. Corp.*, 587 F.3d 1339, 1347 (Fed. Cir. 2009). Based on this "consideration of the context of the rest of the term," and its finding that the term "anhydrous" appeared in the specification "only as a modifier of calcium sulfate," the Federal Circuit rejected a proposed construction that was drawn from an extrinsic dictionary definition. *Id*. Here, the disputed term stands on its own. In *ACTV*, the Federal Circuit rejected a construction that would have imported restrictions with no support in the claim language or specification, and found that the term "uniform resource locator" (URL), "as defined by the language and context of the claims, is something that identifies the location of relevant information segments." *ACTV, Inc. v. Walt Disney Co.*, 346 F.3d 1082, 1088, 1090 (Fed. Cir. 2003).

As discussed above, the intrinsic evidence here shows that the only way memory is measured is in terms of bytes. Accordingly, the Court should construe "portion of the memory" as "number of bytes within the memory."

H. "memory is allocated between the [first] interleaving function and the [second interleaving/ deinterleaving] function"

Plaintiff's Proposed Construction	Defendants' Proposed Construction
"an amount of the memory is allocated to the [first] interleaving function and an amount of memory is allocated to the [second interleaving / deinterleaving] function"	*"a number of bytes of memory are allocated to the [first] interleaving function and a number of bytes of memory allocated to the [second interleaving/ deinterleaving] function"*

1. Plaintiff's Opening Position

The parties agree that this term means that a quantum "of memory is/[are] allocated to the [first] interleaving function and" a quantity of memory "is allocated to the [second interleaving/ deinterleaving] function." However, as with the other terms that reference a quantity of memory, Defendants urge the Court to construe the claim element to limit the quantity of allocation to "a number of bytes." The specification does not require imposition of such a restriction. Defendants' attempt to restrict the scope of this claim element to "number of bytes of memory" is therefore improper.

In contrast to Defendants' unsupported, overly narrowly construction, TQ Delta's proposed construction accounts for the different quantities of memory. The Court should adopt TQ Delta's construction and reject Defendants' construction.

2. Defendants' Answering Position

Here, too, the parties' dispute centers around how memory is measured, as discussed above with respect to "amount of memory" and "portion of the memory." The specification confirms that a number of bytes are allocated. *See, e.g.*, A9 ('890 patent) at 7:50-8:37. As discussed above, there are no "different" measurements of memory disclosed in the specification, and TQ Delta's construction clarifies nothing. The specification explains that "the allocation module 150 allocates a portion of the shared memory 150 to one or more of the interleaver

and/or deinterleavers, or groupings thereof." *See* A8 ('890 patent) at 5:66-6:3. Every example in the specification illustrates allocation in terms of bytes. *See, e.g.*, A6 ('890 patent) at 6:12-14, 6:39-47, 6:26-33; A9 ('890 patent) at 7:11-25, 8:9-19, 8:29-39. Accordingly, the Court should adopt Defendants' proposed construction.

3. Plaintiff's Reply Position

Defendants contend that except for bytes "there are no 'different' measurements of memory disclosed in the specification." This is not true. The specification also recites "bits" and "Kbytes." *See* e.g., A8 ('890 patent) at 5:64 and 6:60. In any event, the sections of the specification that Defendants cite do not constitute "'words or expressions of manifest exclusion or restriction'" that would restrict "memory is allocated" to "a number of bytes of memory are allocated" like Defendants propose. *Innova/Pure Water, Inc. v. Safari Water Filtration Sys.*, 381 F.3d 1111, 1117 (Fed. Cir. 2004) (citing *Liebel–Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004)).

Further, it is incontrovertible that "memory is allocated" is broader than "a number of bytes of memory are allocated." Therefore, even if the specification described embodiments where memory is specified in bytes, it would be improper to restrict the claims to a specific unit of memory i.e., number of bytes "when the claim language is broader than such embodiments." *Electro Med. Sys., S.A. v. Cooper Life Scis., Inc.*, 34 F.3d 1048, 1054 (Fed. Cir. 1994) (noting that "although the specifications may well indicate that certain embodiments are preferred, particular embodiments appearing in a specification will not be read into the claims when the claim language is broader than such embodiments."). The Court should decline to adopt Defendants' construction.

4. Defendants' Sur-reply Position

TQ Delta's argument that the specification measures memory in anything other than bytes is unfounded. TQ Delta omits that the word "bit" is recited in the specification only as "bit error rate," and does not refer to or measure memory. A8 ('890 patent), col. 5:64 ("The parameter determination module 130 then analyzes one or more parameters such as data rate, transmitter data rate, receiver data rate, impulse noise protection, ***bit error rate***, latency, or the like.") (emphasis added). That is not a measurement of memory. And "Kbytes" is, plainly, an amount of bytes measured by the thousands. *See* A636-638, (https://en.wikipedia.org/wiki/Kilobyte (last visited August 22, 2017)).

TQ Delta again relies upon pre-*Phillips* cases in support of its argument that the Court should disregard the repeated and consistent references to memory in terms of "bytes" in the specification. *Supra* at p. 82. As explained above, *Phillips* expressly discouraged the restrictive approach articulated in such cases, because they accorded too little weight to the specification. *Phillips*, 415 F.3d at 1320–21. And in *Electro Med. Sys., S.A. v. Cooper Life Scis., Inc.*, 34 F.3d 1048, 1054 (1994), the Court noted that the construction was correct after looking at the specifications and prosecution histories, as Defendants have done here.

The Court should adopt Defendants' proposed construction for this term.

I. "wherein the generated message indicates how the memory has been allocated between the [first deinterleaving / interleaving] function and the [second] deinterleaving function"

Plaintiff's Proposed Construction	Defendants' Proposed Construction
"wherein the generated message indicates the amount of memory that has been allocated to the [first deinterleaving / interleaving] function and the amount of memory allocated to the [second] deinterleaving function"	*"wherein the generated message indicates a number of bytes of memory allocated to the [first deinterleaving / interleaving] function and a number of bytes of memory allocated to the [second] deinterleaving function"*

1. Plaintiff's Opening Position

The parties agree that "the generated message" indicates the quantity of memory allocated to the "[first deinterleaving / interleaving] function" and the "[second] deinterleaving function." Defendants, however, urge the Court to adopt a construction that limits this quantity of memory to "a number of bytes of memory." There is no basis for this narrow and limiting construction that Defendants urge. While a byte is one measure of memory, the specification does restrict the message to only include an indication that is a function of bytes. As discussed above, an "amount of memory" can be specified in a variety of units and the claims do not dictate use of one type of unit over any others.

On the other hand, TQ Delta's proposed construction – amount of memory – accounts for every possible means of indicating the amount of memory allocated. The Court should adopt TQ Delta's proposed construction.

2. Defendants' Answering Position

The parties dispute whether the generated message specifies a number of bytes of memory. As discussed above, the only purportedly novel aspect of the invention identified during prosecution was a message specifying a maximum number of bytes of shared memory for interleaver and deinterleaver functions. *See* A180 (D.I. 312, Ex. H) (examiner indicating in notice of allowance that point of novelty over prior art was "limiting the memory allocated to the interleaver to a maximum number of bytes available that was specified in a transmitted or received message."). Moreover, as discussed above with respect to "amount of memory" and "portion of the memory," bytes are the only measurement of memory disclosed in the specification.

TQ Delta's proposed construction should be rejected. Again, TQ Delta is transparently trying to broaden the scope of the claims to capture infringement by "different types of

information that can be used to perform the allocation." *Supra* at p. 70. But the intrinsic evidence does not allow for the message to contain "different types of information." The intrinsic evidence very clearly requires that the message "indicates ***how*** the memory has been allocated." A61 ('473 patent) at claim 28. Elsewhere, the specification describes determining "a maximum amount of shared memory that can be allocated to a specific interleaver or deinterleaver," then transmitting "the determined maximum amount" to another transceiver. A9 ('890 patent) at 8:61-67. TQ Delta's assertion that its construction "accounts for every possible means of indicating the amount of memory allocated" underscores just how far divorced from the intrinsic evidence, and the claim language, its proposal is.

The Court should adopt Defendants' proposed construction.

3. Plaintiff's Reply Position

As an initial matter, Defendants' suggestion that the Court should narrow the scope of this element based on statements made by the Examiner in the notice of allowance is without merit. An "examiner's unilateral remarks [do] not alter the scope of the claim." *Salazar v. Procter & Gamble Co.*, 414 F.3d 1342, 1347 (Fed. Cir. 2005); *see also Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1124 (Fed. Cir. 2004) (stating that "[i]t is well settled that it is the applicant, not the examiner, who must give up or disclaim subject matter that would otherwise fall within the scope of the claims."). The Court should reject Defendants attempt to narrow the scope of the claims based on statements made by the Examiner.

Defendants also contend that because allegedly "bytes are the only measurement of memory disclosed in the specification," the contents of the claimed message should be restricted to a number of bytes of memory. First off, there is no basis for Defendants' allegation. The sections of the specification Defendants cite, nowhere even suggest that the contents of the message should be restricted to "a number of bytes." Second, assuming *arguendo* that "bytes are

the only measurement of memory disclosed in the specification," it is nevertheless improper to read the preferred embodiment "into claims when the claim language is broader than such embodiments. *Innova/Pure Water, Inc.*, 381 F.3d at 1117; *Electro Med. Sys., S.A. v. Cooper Life Scis., Inc.*, 34 F.3d 1048, 1054 (Fed. Cir. 1994) (noting that "although the specifications may well indicate that certain embodiments are preferred, particular embodiments appearing in a specification will not be read into the claims when the claim language is broader than such embodiments."). In fact, "even where a patent describes only a single embodiment, claims will not be 'read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using 'words or expressions of manifest exclusion or restriction.'" *Innova/Pure Water, Inc.*, 381 F.3d at 1117 (quoting *Liebel–Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004)). Defendants have not alleged that the patentee has demonstrated a clear intention to limit the scope of the contents of the message to a number of bytes. The Court should reject Defendants' attempt to restrict the scope of this element.

4. Defendants' Sur-reply Position

Faced with evidence that the only purportedly novel aspect of the invention during prosecution was a message specifying a maximum number of bytes of shared memory for interleaver and deinterleaver functions, TQ Delta argues that the prosecution history should be disregarded. TQ Delta's cases do not support ignoring such evidence here. In *Innova/Pure Water*, the Examiner's remarks were disregarded because the Federal Circuit found that after the Examiner made the remarks that were cited in claim construction, the Examiner ultimately allowed the claims unamended after an interview with the applicant, so the "record finally reflect[ed] the examiner's acquiescence to the claim language chosen by the applicant" and there was no clear evidence of any disavowal of claim scope. *Innova/Pure Water*, 381 F.3d at 1124. There is no such evidence here of the examiner's "acquiescence" to the applicant's language. In

Salazar, the Federal Circuit found that the district court erred in finding that an Examiner's remarks "amended" the scope of the "elastic" element of the claim, because "unilateral statements by an examiner do not give rise to a clear disavowal of claim scope by an applicant." *Salazar v. Procter & Gamble Co.*, 414 F.3d 1342, 1347 (Fed. Cir. 2005). Here, the applicant, not the examiner, made the amendments.

TQ Delta again argues, as it has with other terms, that the Court should disregard the specification based on decisions that pre-date *Phillips*. TQ Delta's argument here fails for the same reasons it did with respect to other terms. The Court should adopt Defendants' proposed construction.

VII. CLAIMS ALLEGED AS INDEFINITE UNDER IPXL HOLDINGS

A. Plaintiff's Opening Position

Defendants allege that claim 13 of the '882 patent, claim 19 of the '473 Patent and claims 1 and 10 of the '126 patent are indefinite under *IPXL Holdings, Inc. v. Amazon.com Inc.*, 430 F.3d 1377 (Fed. Cir. 2005). TQ Delta disagrees. The claim at issue in *IPXL Holdings* was found indefinite because it "recite[d] both a system and the method for using that system[.]"[12] *IPXL Holdings, L.L.C. v. Amazon.com, Inc.*, 430 F.3d 1377, 1384 (Fed. Cir. 2005). In contrast, claim 13 of the '882 patent, claim 19 of the '473 Patent and claims 1 and 10 of the '126 patent do not "recite a system and a method for using that system." *Sci. Telecommunications, LLC v. Adtran,*

[12] In *IPXL Holdings*, the Federal Circuit invalidated a claim directed to a 'system of claim 2 [including an input means] wherein ... the user uses the input means to either change the predicted transaction information or accept the displayed transaction type and transaction parameters.' *IPXL Holdings, L.L.C. v. Amazon.com, Inc.*, 430 F.3d 1377, 1384 (Fed.Cir. 2005) (emphasis in original). The Court explained that the claim was indefinite because "it [was] unclear whether infringement ... occurs when one creates a system that allows the user to change the predicted transaction information or accept the displayed transaction, or whether infringement occurs when the user actually uses the input means to change transaction information or uses the input means to accept a displayed transaction." *IPXL Holdings*, 430 F.3d at 1384.

Inc., No. CV 15-647-SLR, 2016 WL 6872311, at *4 (D. Del. Nov. 21, 2016). Instead, claim 19 of the '473 Patent and claims 1 and 10 of the '126 patent recite "a multicarrier communications transceiver that is configured to perform" certain functions. Separately, infringement of claim 13 of the '882 patent does not require that "the user actually use[]" the claimed system. *IPXL Holdings*, 430 F.3d at 1384. For these reasons, *IPXL Holdings* does not apply, and the claims are not indefinite. *Id*.

"[T]he rule established in *IPXL Holdings* has been repeatedly recognized to be a narrow one." *Bayer Pharma AG v. Watson Labs., Inc.*, No. CV 12-1726-LPS-CJB, 2014 WL 4954617, at *6 (D. Del. Sept. 30, 2014); *Sound View Innovations, LLC v. Facebook, Inc.*, No. 16-CV-116, 2017 WL 2221177, at *9 (D. Del. May 19, 2017); *GPNE Corp. v. Apple, Inc.*, Case No.: 12–CV–02885–LHK, 2013 WL 4446819, at *20 (N.D.Cal. Aug. 13, 2013) ("[T]he scope of *IPXL* is very narrow."); *Synqor, Inc. v. Artesyn Techs., Inc.*, No. 2:07–CV–497–TJW–CE, 2010 WL 2991037, at *31 (E.D.Tex. July 26, 2010) ("The [c]ourt agrees with numerous other courts in that the holding in the *IPXL* case is very limited."); *Ricoh Co., Ltd. v. Katun Corp.*, 486 F.Supp.2d 395, 402 (D.N.J. 2007) (explaining that in almost all cases in which a party has argued that *IPXL Holdings* applies to invalidate a claim, the courts have found the rule inapplicable); *Collaboration Props., Inc. v. Tandberg ASA*, No. C 05–01940 MHP, 2006 WL 1752140, at *7 (N.D. Cal. June 23, 2006) (noting that *IPXL Holdings* stands "for [a] narrow rule"). In particular, courts have explained that the rule does not apply to claims containing language simply describing a system as well as the capabilities of the claimed system; rather, the rule applies to claims describing a system that also require the ***user*** of the recited system to take specific action. *See Bayer Pharma AG*, 2014 WL 4954617, at *5 (citing *Microprocessor*

Enhancement Corp. v. Texas Instruments Inc., 520 F.3d 1367, 1374 (Fed. Cir. 2008)) (emphasis added).

Given the narrow scope of *IPXL Holdings*, this Court, like other district courts, has noted that "courts analyzing whether *IPXL Holdings* should apply to invalidate a patent claim must 'focus on whether the claim language is directed to user actions rather than system capabilities.'" *Bayer Pharma AG*, 2014 WL 4954617, at *5 (citing *H–W Tech., LC v. Overstock.com. Inc.*, 973 F.Supp.2d 689, 696 (N.D.Tex. 2013)); *Beneficial Innovations, Inc. v. Advance Publ'ns, Inc.*, No. 2:11–CV–299–JRG–RSP, 2014 WL 186301, at *2 (E.D.Tex. Jan. 14, 2014).

It is incontrovertible that claim 13 of the '882 patent describes a system and claim 19 of the '473 patent and claims 1 and 10 of the '126 patent describe an apparatus. None of these claims on their face "require the user of the recited system[or apparatus] to take specific action" – the hallmark of a claim indefinite under *IPXL Holdings*. *M2M Sols. LLC v. Sierra Wireless Am., Inc.*, No. CV 12-30-RGA, 2016 WL 1298961, at *5 (D. Del. Mar. 31, 2016) (citations omitted). Additionally, there is no hint or indication that "the claim language is directed to user actions rather than system capabilities." *Bayer Pharma AG*, 2014 WL 4954617, at *5. Instead, the claims describe "a system[or apparatus] as well as the capabilities of the claimed system[or apparatus]." Because the claims simply describe the system or apparatus and their capabilities and do not require the user to take specific action, *IPXL Holdings* does not apply to the claim. *See Bayer Pharma AG*, 2014 WL 4954617, at *6 (noting that *IPXL Holdings* "does not apply to claims containing language simply describing a system as well as the capabilities of the claimed system; rather, the rule applies to claims describing a system that also require the user of the recited system to take specific action.") The Court should decline Defendants' invitation to invalidate these claims on this baseless ground.

B. Defendants' Answering Position

As this Court recently recognized, "*IPXL* indefiniteness arises when a person of ordinary skill in the art would be unable to tell if the apparatus itself would infringe or if the apparatus would have to be used in a certain way to infringe." *Sound View Innovations, LLC v. Facebook, Inc.*, No. 16-cv-116, 2017 WL 2221177, at *8 (D. Del. May 19, 2017) (Andrews, J.) (discussing *IPXL Holdings, Inc. v. Amazon.com Inc.*, 430 F.3d 1377, 1384 (Fed. Cir. 2005)). Although *IPXL* addressed a claim that recited both an apparatus and method steps, the Federal Circuit recognized that the reason such claims are indefinite under section 112, paragraph 2 is that they are "not sufficiently precise to provide competitors with an accurate determination of the 'metes and bounds' of protection involved," making it unclear when infringement occurs. *IPXL*, 430 F.3d at 1384 (citation omitted). Thus, the focus of the inquiry is whether a person of ordinary skill in the art would know when infringement occurs, and whether the claim "does not apprise a person of ordinary skill in the art of its scope." *Id*.

Claim 13 of the '882 patent, claims 19 and 28 of the '473 patent, and claims 1 and 10 of the '126 patent are all indefinite under *IPXL*. Claim 13 of the '882 patent is directed to a "system that allocates shared memory" comprising "a transceiver." Then it recites that the transceiver "performs" a list of method steps: "transmitting or receiving a message…", "determining an amount of memory…", "allocating a first number of bytes…", "allocating a second number of bytes…", and "deinterleaving the first plurality of RS coded data bytes…". The use of the present participle ("ing") within the claim indicates the presence of method steps. *Compare Sound View Innovations*, 2017 WL 2221177, at *9 (observing that claim language using "the present participle form of verbs" such as "receiving" and "repeating" is "suggestive of method claiming" and finding claim indefinite under *IPXL*). The system claim's ordered references to transmitting or receiving a message, allocating a first number of bytes, and

allocating a second number of bytes likewise bears the hallmarks of method claiming. *See id*. at *10 (finding that recitation of a "first" message received and a "second" message received indicated "order," as one aspect of method claiming). The first step of the claim recites an apparatus, which would normally indicate that merely buying, using, or selling the apparatus would infringe the claim. The later limitations introduce method steps, such as receiving messages and allocating memory. Viewed by themselves, these would be method steps that would have to be performed in order for the claim to be infringed. Viewed together, it is unclear whether a system with a transceiver itself infringes, or whether the transceiver must be used to perform each of the recited steps to infringe. Thus, this claim is indefinite. *Sound View Innovations,* 2017 WL 2221177, at *8; *IPXL*, 430 F.3d at 1384.

Claim 1 of the '126 patent and claim 19 of the '473 patent also are indefinite because it is unclear when infringement occurs. Both claims are directed to an apparatus comprising "a multicarrier communications transceiver," but later steps recite that the transceiver is "configured to perform" interleaving and deinterleaving functions "wherein the memory is allocated between the [first] interleaving function and the [second interleaving]/ deinterleaving function…" (emphasis added). Thus, it is unclear whether selling a transceiver configured in a certain way is sufficient to find infringement, or whether infringement occurs only when the memory actually "is allocated" in a certain manner. Thus, these claims are indefinite. *Sound View Innovations,* 2017 WL 2221177, at *8; *IPXL*, 430 F.3d at 1384.

Claim 10 of the '126 patent and claim 28 of the '473 patent[13] are both directed to an apparatus comprising a "a multicarrier communications transceiver," but recite that the transceiver is "configured to generate" a message and further recite "wherein the generated

[13] Claim 28 of the '473 patent was inadvertently omitted from the joint claim construction chart, but reflects the same format as claim 10 of the '126 patent.

message indicates how the memory has been allocated between the [first] interleaving function and [the/second] deinterleaving function." (emphasis added). In both sets of claims, when viewed in conjunction with the respective wherein clauses, the "configured to generate" language indicates the performance of a step in a method. Thus, it is unclear whether each claimed apparatus itself infringes, or whether memory must actually have "been allocated" in a certain way to infringe. Accordingly, each of these claims is indefinite as well. *Sound View Innovations,* 2017 WL 2221177, at *8; *IPXL*, 430 F.3d at 1384.

TQ Delta's argument that "user interaction" is required to find a claim indefinite is specious, because the principle invoked under *IPXL* has not been limited to that particular scenario. The Federal Circuit has applied *IPXL* to a claim directed to "a data transmitting device" that recited several buffer and encoding "means" followed by "and transmitting the trellis encoded frames" without any indication of user action. *Rembrandt Data Technologies, LP v. AOL, LLC*, 641 F.3d 1331, 1339 (Fed. Cir. 2011). Finding that "[t]he final element was a method," the Federal Circuit declined to "redraft Rembrandt's claim" and affirmed the district court's indefiniteness ruling. *Id*. at *1339-40; *see also Mastermine Software, Inc. v. Microsoft Corp*., No. 13-cv-0971, 2016 WL 8292205, at *8 (D. Minn. May 6, 2016) (observing that "*Rembrandt* makes clear that a method step is impermissible in a system claim whether performed by a user or by the system itself."). Moreover, *IPXL* itself cited patent office rules that broadly prohibit mixing claim types, regardless of the infringing actor. *See IPXL*, 430 F.3d at 1384 (quoting MPEP § 2173.05(p)(II)) (1999).

The cases TQ Delta relies upon compare user *actions* with system *capabilities.* *H-W Tech* finds a system claim purporting to require user action indefinite because it "creates genuine confusion as to when infringement occurs." *H-W Tech., LC v. Overstock.com, Inc*., 973

F.Supp.2d 689, 697 (N.D. Tex. Sept. 23, 2013). Other cases that TQ Delta relies upon concern limitations that merely specify what a system should be configured to do, and do not contain any ambiguity suggesting that the system might have to actually carry out an action in order for infringement to occur. *See Microprocessor Enhancement Corp. v. Texas Instruments Inc.*, 520 F.3d 1367, 1375 (Fed. Cir. 2008) (finding apparatus claim not indefinite because it was "clearly limited to a pipeline processor possessing the recited structure and *capable* of performing the recited functions" and recognizing that "[t]he conclusion of *IPXL Holdings* was based on the lack of clarity as to when the mixed subject matter claim would be infringed.") (emphasis in original); *Bayer Pharma AG v. Watson Laboratories, Inc.*, No. 12-1726, 2014 WL 4954617, at *8 (D. Del. Sept. 30, 2014) (claim directed to multiphase product comprising several "phase[s]" of "dosage units" was not indefinite where claims did not require actual administration, and where method claim in same patent that did explicitly require user action); *GNPE Corp. v. Apple, Inc.*, 2013 WL 4446819, No. 12-cv-02885, at *19-20 (N.D. Cal. Aug. 13, 2013) (limitation directed to "an interface controlled by the least one processor to" transmit or receive signals not indefinite under *IPXL* because the "to" language simply "provide[d] additional information regarding the structure of the 'node' by describing the node's functionality."); *Synqor, Inc. v. Artesyn Techs., Inc.*, No. 2:07-cv-497, 2010 WL 2991037, at *31 (E.D. Tex. July 26, 2010) (claim term "is not driven into saturation" merely described structure and capabilities of claimed "non-regulating isolating step-down DC-DC power converter"); *Ricoh Co. v. Katun Corp.*, 486 F.Supp.2d 395, 403 (D.N.J. May 3, 2007) (preamble directed to a "lid to selectively plug or unplug a discharge mouth of a developer container mounted to an image forming apparatus for replenishing a developer" found to be a functional description of lid whose structure is further described in body of claim); *Collaboration Properties, Inc. v. Tandberg ASA*, No. C 05-01940,

2006 WL 1752140, at *5-7 (N.D. Cal. June 23, 2006) (system claim "configured to reproduce images" not indefinite because it recited system capabilities); *Beneficial Innovations, Inc. v. Advance Publications, Inc*., No. 2:11-cv-229, 2014 WL 186301, at *4 (E.D. Tex. Jan. 14, 2014) (limitations in apparatus wherein information is used for determining that a network transmission will be processed in a predetermined expected manner not indefinite because they "do not require actions" but instead "inform a person of ordinary skill how the claimed apparatus should be constructed."); *M2M Sols. LLC v. Sierra Wireless Am., Inc*., No. 12-30-RGA, 2016 WL 1298961, at *5 (D. Del. Mar. 31, 2016) ("wherein the processing module authenticates" simply "describes how the processing module itself performs its recited authenticating function").

Here, as discussed above, it is unclear whether the claimed apparatuses themselves infringe, or whether something more than system capabilities are required. Accordingly, it would be unclear to a person of ordinary skill in the art when infringement occurs, and this Court should find claim 13 of the '882 patent, claims 19 and 28 of the '473 patent and claims 1 and 10 of the '126 patent indefinite under *IPXL*.

C. Plaintiff's Reply Position

It is incontrovertible that "*IPXL* is a narrow rule." *Sound View Innovations, LLC v. Facebook, Inc.*, No. 16-CV-116 (RGA), 2017 WL 2221177, at *9 (D. Del. May 19, 2017). "Subsequent decisions by the Federal Circuit upheld this rule [to invalidate a claim] where, as in *IPXL*, the claim language expressly required both an apparatus and that a user actually use the apparatus." *M2M Sols. LLC v. Sierra Wireless Am., Inc.*, No. CV 12-30-RGA, 2016 WL 1298961, at *4 (D. Del. Mar. 31, 2016) (citing *H-W Tech., L.C. v. Overstock.com, Inc.*, 758 F.3d 1329, 1336 (Fed. Cir. 2014) and *In re Katz Interactive Call Processing Patent Litig.*, 639 F.3d 1303, 1318 (Fed. Cir. 2011)). "[T]he rule does not apply to claims containing language simply describing a system as well as the capabilities of the claimed system; rather, the rule applies to

claims describing a system that also require the user of the recited system to take specific action." *Bayer Pharma AG v. Watson Labs., Inc.*, No. 12-1726-LPS-CJB, 2014 WL 4954617, at *6 (D. Del. Sept. 30, 2014) (citing various district court opinions in accord with this position).

Defendants apparently concede, because they do not attempt to prove otherwise, that the claims do not expressly require "the user of the recited system to take specific action." This should doom Defendants' challenge. Nevertheless, citing *Rembrandt Data Technologies, LP v. AOL, LLC*, 641 F.3d 1331, 1339 (Fed. Cir. 2011), Defendants argue that invalidity under *IPXL* does not require "both an apparatus and that a user actually use the apparatus." *Rembrandt* is inapposite. In *Rembrandt*, the claim[14] at issue recited "[a] data transmitting device . . . , comprising: first buffer means for partitioning said stream into frames ... and *transmitting the trellis encoded frames*." *Mastermine Software, Inc. v. Microsoft Corp.*, No. 13-CV-0971 (PJS/TNL), 2016 WL 8292205, at *7 (D. Minn. May 6, 2016) (citing *Rembrandt Data Technologies, LP*, 641 F.3d at 1339). The claim in *Rembrandt* was held invalid because the first four elements recited apparatus elements and the final element recited use of the apparatus for *transmitting the trellis encoded frames. Rembrandt Data Technologies, LP*, 641 F.3d at 1339.

[14] The claim at issue in *Rembrandt* recites:

A data transmitting device for transmitting signals corresponding to an incoming stream of bits, comprising:

first buffer means for partitioning said stream into frames of unequal number of bits and for separating the bits of each frame into a first group and a second group of bits;

fractional encoding means for receiving the first group of bits of each frame and performing fractional encoding to generate a group of fractionally encoded bits;

second buffer means for combining said second group of bits with said group of fractionally encoded bits to form frames of equal number of bits; trellis encoding means for trellis encoding the frames from said second buffer means; and

transmitting the trellis encoded frames.

Rembrandt Data Techs., 641 F.3d at 1339.

None of the claims at issue mix "apparatus elements" with use of the apparatus to perform a method step. The claims do not run afoul of *IPXL*.

Defendants also cite to *Sound View Innovations* to support their contention that the claims are invalid under *IPXL*. *Sound View Innovations* does not support Defendants, however. In *Sound View Innovations*, this Court invalidated a claim because "the claim language beg[ged] its application for five reasons." *Sound View Innovations, LLC v. Facebook, Inc.*,, No. 16-CV-116 (RGA), 2017 WL 2221177, at *9 (D. Del. May 19, 2017). None of the claims here suffer from any of the infirmities identified in *Sound View Innovations* much less all five of the reasons. In particular, unlike the claim in *Sound View Innovations*, none of the claims here are alleged to recite elements that "transition from the present form of the verb . . . to the present participle form[.]" *Sound View Innovations, LLC.*, 2017 WL 2221177, at *10. Also, unlike the claim in *Sound View Innovations*, none of claims here have "order and repetition, the province of method claiming" as noted by the *Sound View* Court. *Id*. Defendants make much of the fact that certain claims use the present participle form of verbs. As this Court noted, however, "[u]se of the present participle form does not "automatically convert the claims into method claims." *Sound View Innovations, LLC*, 2017 WL 2221177, at *9 (quoting *Leader Techs v. Facebook, Inc.*, 770 F. Supp. 2d 686, 707 (D. Del. 2011)).

Each of the claims at issue describes a system or apparatus as well as the capabilities of the claimed system or apparatus. Claims such as these pass muster under *IPXL*. *Bayer Pharma AG.*, 2014 WL 4954617, at *6; *see also*, *Edgewell Pers. Care Brands, LLC v. Albaad Massuot Yitzhak, Ltd.*, No. CV 15-1188-RGA, 2017 WL 1900736, at *5 (D. Del. May 9, 2017) (noting that "[t]he phrase 'being inserted into said body' explains a characteristic of how the tapered tip provides contact and support" and that the "phrase does not require user action.").

None of the claims at issue here "suggest[] the need for user action." *Edgewell Pers. Care Brands, LLC.*, 2017 WL 1900736, at *5. Instead each describes a system or apparatus as well as the capabilities of the claimed system or apparatus. Accordingly, on their face, the claims are readily distinguishable from *IPXL*.

For at least the foregoing reasons, the claims are not invalid under *IPXL*.

D. Defendants' Sur-reply Position

Claim 13 of the '882 patent, claims 19 and 28 of the '473 patent, and claims 1 and 10 of the '126 patent are indefinite under *IPXL*. General statements characterizing *IPXL* as "narrow" do not diminish the fundamental principle that claims must be sufficiently clear to apprise a person of ordinary skill in the art of their metes and bounds. *See IPXL Holdings, Inc. v. Amazon.com Inc.*, 430 F.3d 1377, 1384 (Fed. Cir. 2005); *Sound View Innovations, LLC v. Facebook, Inc.*, No. 16–cv–116 (RGA), 2017 WL 2221177, at *1 (D. Del. May 19, 2017). Indeed, after *IPXL* issued, the Supreme Court confirmed the critical public notice function of Section 112, Paragraph 2. *See Nautilus, Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120, 2130 (2014) (warning against "diminish[ing] the definiteness requirement's public-notice function" and "foster[ing] the innovation-discouraging zone of uncertainty against which this Court has warned") (citation and internal quotation marks omitted).

In attempting to avoid indefiniteness under *IPXL*, TQ Delta tries to distinguish between user actions and system actions. But neither *IPXL* nor its progeny support such a distinction. *See supra* at pp. 92-94 (distinguishing *H-W Tech.*, *Bayer Pharma AG*, and *M2M Sols. LLC*); *Edgewell Pers. Care Brands, LLC v. Albaad Massuot Yitzhak, Ltd.*, C.A. No. 15–1188–RGA, 2017 WL 1900736, at *5 (D. Del. May 9, 2017) (finding that phrase related to system capabilities rather than user action); *In re Katz Interactive Call Processing Patent Litig.*, 639 F.3d 1303, 1318 (Fed. Cir. 2011) (finding that 'wherein' clause requiring that callers 'digitally

enter data' "is directed to user actions not system capabilities" and therefore rejecting patentee's argument that "does not signify a method step but instead defines a functional capability")). The key distinctions the courts there made were between *actions* (*i.e.*, a method step) and *capabilities* (*i.e.*, an element of an apparatus). If an apparatus claim recites a method step— whether it is the system or a user that must perform the action—the claim is still indefinite. *See InterDigital Commn's, Inc. v. ZTE Corp.*, C.A. No. 1:13-cv-000009-RGA, 2014 WL 1620733, at *5 (D. Del. Apr. 22, 2014) (noting that the Court would not "rewrite a method step in an apparatus claim to preserve its validity" and holding the claim indefinite).

TQ Delta attempts to distinguish *Rembrandt* on the basis that the claims recited "apparatus elements" where the final element was a method step (reciting the present participle "transmitting"). But the *Rembrandt* court did not ascribe any significance to the means-plus-function format of the claim. Instead, the *Rembrandt* court found that "reciting both an apparatus and a method of using that apparatus renders a claim indefinite." *Rembrandt Data Techs., L.P. v. AOL, LLC*, 641 F.3d 1331, 1339 (Fed. Cir. 2011); *see also Mastermine Software, Inc. v. Microsoft Corp.*, C.A. No. 13–CV–0971 (PJS/TNL), 2016 WL 8292205, at *8 (D. Minn. May 6, 2016) ("Rembrandt makes clear that a method step is impermissible in a system claim whether performed by a user or by the system itself.").

Absent from TQ Delta's discussion of the *Rembrandt* decision is any discussion of the claims at issue here. The asserted claims suffer from the same fundamental defect as the claim that was invalidated by the court in *Rembrandt, i.e.,* one of ordinary skill in the art would not know when the claim was infringed. In *Rembrandt*, the claim was drawn to a "data transmitting device" comprising a first buffer means, a fractional encoding means, and a second buffer means – all device limitations. *See Rembrandt*, 641 F.3d at 1339. The final limitation recited a method

step, "transmitting the trellis encoded frames." *Id.* In *Rembrandt*, one of ordinary skill would not have known whether the claim was infringed when the device was sold, or when the trellis-encoded frames were actually transmitted.

Claim 19 of the '473 patent suffers from the same flaw. It is reproduced here:

> 19. An ***apparatus*** comprising:
> ***a multicarrier communications transceiver*** that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path, the multicarrier communications transceiver being associated with a memory,
> wherein the ***memory is allocated*** between the interleaving function and the deinterleaving function ***in accordance with a message received during an initialization*** of the transceiver and wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.

A61 ('473 patent), col. 11:39-52 (emphasis added).[15] The claim recites an apparatus, "a multicarrier communications transceiver," but later steps recite "wherein the memory ***is allocated*** between" interleaving and deinterleaving functions in accordance with a message "received ***during*** initialization of the transceiver." The claim recites an apparatus, but also indicates that the invention requires allocating memory in accordance with a message received during initialization. This implies that the message must have been received, and the memory must have been allocated according to the message to practice the invention. One of ordinary skill in the art would not know whether infringement occurred merely by owning the transceiver, or if the memory must be allocated in advance, or already allocated when sold, to infringe.

Claim 10 of the '126 patent and claim 28 of the '473 patent similarly recite an apparatus, "a multicarrier communications transceiver," that is "configured to generate a message." The

[15] Claim 1 of the '126 patent is very similar to claim 19 of the '473 patent, but recites a first and second interleaving function, as opposed to an interleaving function and a deinterleaving function. *See* A73 ('126 patent), col. 10:43-56. Claim 1 of the '126 patent has the same problem as claim 19 of the '473 patent, and should be invalidated for the same reason.

generated message, however, "indicates how the memory ***has been allocated***" according to a message between interleaving and deinterleaving functions, which recites that the memory has been allocated at some point before the transceiver was operating. Again, one of ordinary skill in the art would not know when this claim was infringed, thus the claim is indefinite.

Claim 13 of the '882 patent recites a "system that allocates shared memory" comprising a "transceiver," then recites a number of method steps performed by the transceiver. A35 ('882 patent), col. 12:19-43. Claim 13 does not recite language of capability as TQ Delta argues. And as in *Rembrandt*, one of ordinary skill would not know if a transceiver itself infringed, or if the transceiver must perform the method steps to infringe.

TQ Delta also argues that the claims cannot be indefinite because the claims here do not invoke "all five of the reasons" this Court found indefiniteness in *Sound View Innovations*. *Supra* at p. 96. But *Sound View Innovations* did not purport to establish a five-part test. Instead, *Sound View Innovations* confirms that the *IPXL* analysis is fact-specific. TQ Delta focuses on the language of the claims in other cases such as *Rembrandt*, and then asserts that the claims at issue here are not indefinite because each "describes a system or apparatus as well as the capabilities of the claimed system or apparatus" (*Supra* at p. 96). But TQ Delta does not analogize or draw any parallels from the claims in those cases to the claims at issue here, and points to no specific language in any of the asserted claims that clarifies when infringement occurs.

Because it would be unclear to a person of ordinary skill in the art when infringement occurs, this Court should find claim 13 of the '882 patent, claims 19 and 28 of the '473 patent, and claims 1 and 10 of the '126 patent indefinite under *IPXL*.

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Respectfully submitted,

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